Ontwerp van 10Gb/s-burstmodeontvangers voor passieve optische netwerken met hoge splitfactor en groot bereik

Design of 10 Gb/s Burst-Mode Receivers for High-Split Extended Reach PONs

Tine De Ridder

Promotoren: prof. dr. ir. J. Vandewege, prof. dr. ir. X.-Z. Qiu
Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Informatietechnologie
Voorzitter: prof. dr. ir. D. De Zutter
Faculteit Ingenieurswetenschappen
Academiejaar 2009 - 2010

UNIVERSITEIT GENT

ISBN 978-90-8578-353-4
NUR 959
Wettelijk depot: D/2010/10.500/29

Voor bompa

Dankwoord

Dit proefschrift is het resultaat van meer dan 5 jaar studie en onderzoek als medewerker van imec en de Universiteit Gent. Ik wens dan ook mijn waardering uit te drukken voor prof. dr. ir. Paul Lagasse en prof. dr. ir. Daniël De Zutter, respectievelijk vorig en huidig voorzitter van de vakgroep Informatietechnologie. Ik wens hen te bedanken voor de aangeboden faciliteiten en voor de perfecte omkadering die voorzien wordt in de vakgroep.

Mijn speciale dank gaat uit naar prof. dr. ir. Jan Vandewege en prof. dr. ir. Xing-Zhi Qiu, de promotoren van dit proefschrift, voor de deskundige begeleiding, het vertrouwen, de vele creatieve ideeën en de ongedwongen en stimulerende werksfeer, waarin ik mij steeds heb thuis gevoeld. Verder dank ik hen ook voor het grondig nalezen van de tekst.

Ik bedank Bjorn Vandecasteele (ELIS) en Liesbet Van Landschoot (Photonics Research Group) voor het toevoegen van bond wires in de 10 G PIN-TIA module, het uitvoeren van de FIB-operatie op de 10 G TIA en het nemen van foto's van de module.

Verder wens ik de collega's van de INTEC_designgroep te bedanken voor de aangename samenwerking gedurende deze jaren. Jullie hebben allemaal wel op de een of andere manier bijgedragen aan het behalen van mijn doctoraat. In het bijzonder wens ik prof. dr. ir. Johan Bauwelinck, ir. Cedric Mélange en ir. Bart Baekelandt te bedanken voor de vele interessante discussies. Mijn speciale dank gaat ook uit naar dr. ir. Xin Yin voor het uitvoeren van de vele metingen, maar vooral voor de motivatie tijdens moeilijke momenten. Daarnaast bedank ik ook Jan Gillis voor de vele technische interventies op mijn computer, het soldeerwerk en de fabricage van verschillende bordjes.

Naast collega's zijn ook vrienden onontbeerlijk tijdens het doctoraatsproces. Bedankt aan al diegenen die voor voldoende afleiding gezorgd hebben de laatste jaren. Vooral de mensen van Kalliope hebben hun steentje bijgedragen met de ontelbare fantastische (zang)momenten en onvergetelijke concerten. Ik bedank Peter Ossieur voor de zeer uitgebreide opleiding tot chipontwerper. Daarnaast wist je me steeds opnieuw te motiveren ook al waren vele situaties tijdelijk uitzichtloos.

Ik bedank ook mijn vader omdat hij nooit heeft opgegeven om mij richting ingenieurswetenschappen te pushen. Ik ken nu eindelijk het antwoord op de vraag 'vake, wat doet een ingenieur?'. Mijn moeder zorgde voor de emotionele steun in

moeilijke momenten. Ook mijn broers stonden steeds klaar om mij te motiveren. Tot slot bedank ik ook mijn grootouders voor de financiële steun en de continue interesse in mijn doctoraatswerk.

Gent, maart 2010

Tine De Ridder

Table of Contents

List of Figures

List of Tables

Glossary

3R reamplification, regeneration and retiming.

ADSL asymmetric digital subscriber line.

AGC automatic control loop.

APD avalanche photodiode.

ASE amplified spontaneous emission.

ASIC application specific IC.

AUTOFUN 'Fiber Optic Transceivers for Automotive Infotainment Networks'.

AWG arrayed waveguide.

B2B back-to-back.

BER bit error ratio.

BJT bipolar junction transistor.

BM burst-mode.

BM-PA burst-mode post-amplifier.

BM-Rx burst-mode receiver.

BM-TIA burst-mode transimpedance amplifier.

CAD computer aided design.

CAPEX capital expenditure.

CATV cable television.

CDR clock and data recovery.

CE common emitter.

CID consecutive identical digits.

CML current-mode logic.

CMRR common-mode rejection ratio.

CW continuous wave.

CW-CDR continuous-mode CDR.

CW-Rx continuous-mode receiver.

DCF dispersion compensating fiber.

DCM dispersion compensating module.

DDLA differential difference limiting amplifier.

DEC decision circuit.

DFB-LD distributed feedback laser laser diode.

DR dynamic range.

DWDM dense WDM.

EAM Electro-Absorption Modulator.

ECL emitter-coupled logic.

EDC electronic dispersion compensation.

EDFA erbium doped fiber amplifier.

EMI electromagnetic interference.

ER extinction ratio.

FEC forward error correction.

FIB focussed ion beam.

FSAN Full Service Access Network.

FTTB fiber-to-the-building.

FTTC fiber-to-the-curb.

FTTH fiber-to-the-home.

FTTx fiber-to-the-x.

HBT heterojunction bipolar transistor.

HD high definition.

HDSL high bit-rate digital subscriber line.

HF high-frequency.

HFC hybrid fiber coax.

I/O input/output.

IC integrated circuit.

IDAC current digital to analog converter.

IEEE Institute of Electrical and Electronical Engineers.

ISI intersymbol interference.

ISO isolator.

ITU-T International Telecommunications Union.

LA limiting amplifier.

LE local exchange.

LPF low-pass filter.

MAC medium access control.

MARISE 'Materials for Avalanche Receiver for ultImate SEnsitivity'.

MLF Micro Lead Frame.

MOST Media Oriented Systems Transport.

MZI Mach-Zehnder Interferometer.

NRZ non-return to zero.

OBPF optical bandpass filter.

ODN optical distribution network.

OLT optical line termination.

ONU optical network unit.

OPEX operational expenditure.

OSNR optical SNR.

OTA operational transconductance amplifier.

P2MP point-to-multipoint.

P2P point-to-point.

PA post-amplifier.

PCB printed circuit board.

PCS plastic cladded silica.

PD photodetector.

PIEMAN 'Photonic Integrated Extended Metro and Access Network'.

PKD peak detector.

POF plastic optical fiber.

PON passive optical network.

PRBS pseudo-random bit sequence.

PSD power spectral density.

PSRR power supply rejection ratio.

PWD pulse width distortion.

Rx receiver.

SE2Diff Single-ended to differential converter.

SME small and medium sized enterprises.

SN service node.

SNR signal-to-noise ratio.

SOA semiconductor optical amplifiers.

TDMA time division multiple access.

THE threshold extraction.

TIA transimpedance amplifier.

Tx transmitter.

UCC University College Cork.

UGA unity gain amplifier.

VDSL very high-speed DSL.

VOA variable optical attenuator.

VPN virtual private network.

xDSL x-digital subscriber line.

XG-PON Next Generation PON.

Nederlandse Samenvatting –Summary in Dutch–

In het laatste decennium zijn er verscheidene nieuwe internettoepassingen opgedoken, die meer en meer gegevens over het netwerk versturen. Het succes van deze toepassingen wordt grotendeels bepaald door de beschikbaarheid van breedbandnetwerkverbindingen. Om in de toekomst nieuwe toepassingen blijvend te kunnen ondersteunen zijn snellere internetverbindingen onontbeerlijk. In het verleden hebben de internetoperatoren de bestaande koperen infrastructuur van het telefoonnetwerk en het televisiedistributienetwerk herbruikt. Dit heeft een aantal nadelen. De bandbreedte van deze koperen kabels is beperkt en door de hoge verliezen zijn veel versterkers nodig. Dit leidt tot netwerken die veel vermogen verbruiken. De toekomst van breedbandinternetverbindingen ligt dan ook in het gebruik van de optische vezel als transmissiemedium. De optische vezel heeft een vrijwel onbeperkte bandbreedte en door de lage verliezen kunnen langere afstanden overbrugd worden. Hierdoor zijn minder schakelcentrales en versterkers nodig wat dit netwerk een stuk groener maakt dan de kopergebaseerde netwerken.

Voor deze doctoraatsthesis werd een ontvanger ontworpen voor 10 Gb/s optische toegangsnetwerken. Het netwerk zelf werd voorgesteld in het door de Europese Unie ondersteunde FP6 IST-project PIEMAN (Photonic Integrated Extended Metro and Access Network). In dit netwerk worden optische versterkers gebruikt om afstanden tot 100 km te overbruggen en een hoger aantal gebruikers te voorzien op eenzelfde centraal knooppunt. Het netwerk biedt een 10 Gb/s verbinding aan zowel in de zend- als ontvangstrichting.

De pakketjes van de verschillende gebruikers komen via een apart toegangsnetwerk met aparte vezels via een optische koppelaar op één vezel terecht. Hiervoor wordt het TDMA (time division multiple access protocol)-protocol gebruikt. Omdat niet elke gebruiker zich op dezelfde (vezel)afstand van de optische koppelaar bevindt, komt elk pakketje met een andere sterkte toe bij de ontvanger. Om deze snelle opeenvolging van pakketjes met sterk verschillend vermogen correct te ontvangen is een zogenaamde burstmodeontvanger nodig. Vergeleken met een ontvanger voor continue gegevenstransmissie, die een continue stroom van even sterke pakketjes ontvangt, is het ontwerp van burstmodeontvangers veel complexer. De specifieke vereisten aan de ontvanger zijn:

- het correct ontvangen van zowel sterke als zwakke pakketten
- het omvormen van de ontvangen gegevens tot signalen met logische niveaus

- detectie van de start van het binnenkomende pakket
- detectie van het einde van het binnenkomende pakket
- het instellen van de pakketafhankelijke versterking en het pakketafhankelijke beslissingsniveau
- de ingestelde versterking en het ingestelde beslissingsniveau wissen in de korte tijd tussen de pakketten.

Tijdens het ontwerp van de burstmodeontvanger kwam er nog een extra moeilijkheid gerelateerd aan de hoge snelheid aan het licht. Aan 10 Gb/s kan men de invloed van de parasitaire capaciteit en inductanties niet meer verwaarlozen. Deze inductanties en capaciteiten geven aanleiding tot resonanties binnen de bandbreedte van de ontvanger. Deze resonanties hebben invloed op de stabiliteit en de transfertfunctie van de ontvanger wat kan leiden tot desastreuze intersymboolinterferentie. Daarom hebben we de verpakking en parasitaire elementen van de fotodiode gemodelleerd en al vanaf de ontwerpsfase van de circuits in beschouwing genomen.

Het voorgestelde doctoraat behandelt de architectuurstudie en het ontwerp van zowel een burstmodetransimpedantieversterker als een burstmodebegrenzende versterker werkende aan 10 Gb/s. Deze twee chips zijn de twee meest kritische onderdelen van de burstmodeontvanger. De transimpedantieversterker vormt de stroom van de fotodiode om tot een differentiële uitgangsspanning. De begrenzende versterker converteert deze signalen vervolgens tot de gewenste logische niveaus. Om aan de strenge vooropgestelde vereisten te voldoen, stellen we de transimpedantieversterking in aan het begin van het pakket en dit afhankelijk van de sterkte van het binnenkomende pakket. Een systeem om de versterking te vergrendelen vermijdt dat de versterking wijzigt tijdens het ontvangen van de gegevens zelf. Dit werd gedaan omdat zo'n verandering van versterking tijdens het ontvangen van de gegevens zou leiden tot het foutief ontvangen van de rest van het pakket. Het volledige pakket zou dus opnieuw verzonden moeten worden. Op de transimpedantieversterkerchip wordt er ook een ruw beslissingsniveau geëxtraheerd. Dit zorgt voor een groter dynamisch bereik. Voor de begrenzende versterker werd een feed-forward architectuur bestaande uit 4 trappen gekozen. Hierna volgt nog een uitgangsbuffer om de totale versterking op te drijven. Er werd een systeem ontworpen dat het einde van het pakket detecteert. Dit systeem genereert een puls die gebruikt wordt om alle instellingen eigen aan het net ontvangen pakket te verwijderen zowel op de transimpedantieversterker als op de begrenzende versterker. Ook de start van het pakket wordt gedetecteerd door de begrenzende versterker zelf. Dit heeft tot gevolg dat de ontvanger geen externe tijdskritische signalen meer nodig heeft.

De gekozen technologie en de bijbehorende voedingsspanningsbeperking vereiste creativiteit bij de implementatie van de piekdetectoren op beide chips. De traditioneel gebruikte piekdetectoren gebruiken bipolaire transistoren in diodeconfiguratie. Tijdens het detecteren van de piek staat de diode voorwaarts gepolariseerd en de stroom die hij voert wordt gebruikt om de capaciteit op te laden

tot de piekspanning. Nadat deze piekspanning bereikt is, staat de diode gesperd. Door de extra dopering van de bipolaire transistoren in de gebruikte technologie is het niet toegelaten om deze als diode geschakelde bipolaire transistoren gesperd te gebruiken. Dit veelvuldig sperren zou een degradatie van de voorwaartse stroomversterking tot gevolg hebben. Om dit probleem op te lossen hebben we stroomgeschakelde piekdetectoren ontworpen. Het ontwerp en de nadelen van dit type piekdetector worden uitvoerig beschreven in deze doctoraatsthesis.

Dit zijn de voornaamste bijdragen van de auteur, die in dit werk beschreven zijn: 1) architectuurstudie van de transimpedantieversterker; 2) ruisoptimalisatie van de voorversterker; 3) ontwerp van het systeem om de transimpedantieversterking te fixeren aan het begin van het pakket; 4) ontwerp van het circuit dat het einde van het pakket detecteert; 5) architectuurstudie van de begrenzende versterker; 6) geïntegreerd circuitontwerp van de meest kritische circuits op de burstmodetransimpedantieversterker en van de volledige burstmodebegrenzende versterker.

De resultaten van deze onderzoeksinspanningen werden erkend door imec, door UGent en door de projectpartners. Dit onderzoek leidde tot een internationale octrooiaanvraag getiteld 'Device and method for signal detection in a TDMA network' in 2009.

English Summary

The continuous stream of new applications for the internet, increases the need for higher access speed in the currently deployed communication networks. Most networks in use today still consist of twisted copper wires, inherited from the telephone network. The disadvantages of reusing the existing telephone network are twofold. Firstly, the bandwidth of twisted copper wires is limited and secondly, a large number of switches and routers are needed throughout the network leading to an excessive power consumption. The hybrid fiber coax network that reuses the television distribution network is not free from these drawbacks. The bandwidth is also limited and power hungry amplifiers are needed to bridge the distance to and from the user. The future of broadband access lies in optical fiber networks. The optical fiber has a virtually unlimited bandwidth and the lower attenuation leads to less switches and amplifiers in the network, reducing the power consumption of the complete infrastructure.

This dissertation describes the design of a 10 Gb/s burst-mode receiver for high-split extended reach passive optical networks (PONs). The burst-mode receiver was designed within the EU-funded FP6 IST project PIEMAN (Photonic Integrated Extended Metro and Access Network) in which a new network architecture was proposed. In this network, the total power consumption is reduced by incorporating the traditionally separate access and metro parts of the communication network into one network infrastructure and optimizing the resulting complete architecture. At the same time, the data rate is increased to 10 Gb/s. This new network would have a reduced complexity resulting in cheaper and more efficient operation. It can connect up to 512 users per wavelength channel over 100 km by means of dense wavelength division multiplexing, the time division multiple access protocol and optical amplification. For the first time a data rate of up to 10 Gb/s would be available both in upstream and downstream.

The PIEMAN network uses the TDMA (time division multiple access) protocol in the upstream direction requiring burst-mode receivers. These receivers are different to continuous mode receivers because the data stream received by both receivers is totally different. In the case of a continuous receiver, the received data is a continous stream of packets, with a constant signal strength. A burst-mode receiver has to be designed to deal with a quick succession of packets all with a different strength. The time between packets is unknown but can be as short as only a few hundred bits. This data stream obviously puts stringent requirements on the burst-mode receiver, making it a lot more challenging to design than the continuous receiver. The burst-mode receiver's requirements are:

- receive both very strong bursts and very weak bursts correctly
- transform the incoming optical data to output data with logical levels
- detect the start of the incoming burst
- detect the end of the incoming burst
- prepare the receiver for the next burst during the short burst interval
- quickly set the receiver's gain and threshold within a few hundred bits at the beginning of the burst.

The designed receiver incorporates two very advanced features. Firstly, the burst-mode receiver locks its gain setting within 6 ns avoiding packet loss due to gain switching during data payload reception. Secondly, the burst-mode receiver detects both burst start and burst end, making it the first burst-mode receiver of its kind to operate without any time critical signal requirements from outside the burst-mode receiver.

Extra challenges are related to the high-speed design at 10 Gb/s. The influence of the packaging parasitics is no longer negligible at these high speeds. The bond wire inductances combined with the packaging capacitances give rise to resonance peaks within the receiver's bandwidth. These resonances effect the stability and transfer function of the receiver leading to detrimental intersymbol interference. Therefore, the packaging of the dies, including the photodetector's parasitics, was modeled and included into the circuit design phase to avoid these negative effects.

The presented work covers the chip-level architecture study and design of a 10 Gb/s burst-mode transimpedance amplifier and a 10 Gb/s post-amplifier, which are the two most critical components of a burst-mode receiver. The transimpedance amplifier converts the photocurrent into a differential output voltage and the post-amplifier transforms this data to the logical levels required. To fulfill the requirements, we decided to switch the transimpedance gain at the beginning of the burst. To avoid switching the gain during data, which would lead to loss of burst, the gain is locked very soon into the burst. A coarse threshold is extracted to achieve a larger dynamic range. For the post-amplifier, we have chosen a multistage feedforward architecture to cope with the strong timing requirements. It consists of 4 gain stages with threshold extraction and an output buffer with extra gain. To simplify the interface between physical layer and medium access control (MAC) layer, we designed a system that detects the end of the burst. A reset signal is generated when this burst end is detected. This reset is then used to erase all information of the previous burst. The post-amplifier also detects the start of the burst. These advanced features imply that the burst-mode receiver can also operate in nodes where no MAC layer is present.

The selected technology (0.25 μm SiGe BiCMOS) and its maximum supply voltage of 2.5 V also posed additional challenges related to the implementation of peak detectors. Traditionally, these peak detectors use a bipolar transistor in diode configuration. During the detection of the peak, this diode is forward biased

and conducts current charging the peak detector capacitance. When the peak has been acquired, the diode is reverse biased. The reverse biasing of diode configurated bipolars was not allowed in the used technology due to current degradation. A current switched peak detector was designed as a new implementation for the peak detectors. The design and drawbacks of this type of peak detector will be extensively covered in this thesis.

The major contributions of the author in this work are: 1) architecture study of transimpedance amplifier; 2) noise optimization of the front-end; 3) design of a gain locking system to avoid burst loss; 4) design of reset detection circuit; 5) architecture study of post-amplifier; 6) integrated circuit design of the most critical circuits on the burst-mode transimpedance amplifier and the complete burst-mode post amplifier.

The achievements obtained in this research work have been recognized by imec, UGent and the project partners. The research lead to a patent application on 'Device and method for signal detection in a TDMA network' in 2009.

Een akkoord zonder grondnoot is als
een ladder zonder onderste trede.

Sabine Haenebalcke

1 Introduction

1.1 Background

Since the internet became publicly available early 1990s its user number has exponentially grown and it has now become a commonality and access to it has even become a right. Initially, the information was transported over the twisted pair copper lines and within the bandwidth intended for voice transport. The data rate was limited to 56 kb/s, which was just enough for supporting email and chat applications along with very simple websites. About 20 years on, new applications have been continuously emerging, each application demanding more bandwidth, driving the evolution of access network technologies. Thanks to access network technologies like x-digital subscriber line (xDSL) which have higher data rate capabilities, websites could provide more and more graphical content along with media content. Today, core/metro networks support data rates of over 100 Gb/s [1] and the maximum download and upload speeds are limited at a lower data rate by the connection between user and the core/metro network. The connection between this high-speed long-haul core/metro network and the end user is traditionally called an access network. The main cost of a network is the installation cost. So it was evident that telecom operators reused the existing copper networks for providing broadband access. With a maximum downstream data rate of 52 Mbps, very high-speed DSL (VDSL) pushes the speed boundries of twisted copper pair access. The maximum range of a VDSL line however is limited to a mere 1 km. With typical subscriber to local exchange (LE) distances of up to 10 km, xDSL

requires a lot of fiber-fed street cabinets. When using asymmetric digital subscriber line (ADSL) and high bit-rate digital subscriber line (HDSL) the data rate should be reduced if the user is located further away from the street cabinet. In twisted pair access networks, the maximum bandwidth-distance product is limited by losses of the network and dispersion, and by crosstalk between the line pairs of a common cable. Another popular access technology based on existing cable television (CATV) wiring, is called hybrid fiber coax (HFC) network. Initially installed to provide one-directional broadcast services, most CATV networks now use part of the available +/- 1 GHz bandwidth to provide bidirectional communication services over a maximum distance of about 100 km. The bandwidth however is shared between users and is not sufficient for novel applications like high definition (HD) television, video on demand, network gaming, ... Obviously, there is a need for a new access technology with much higher bandwidth to enable future applications.

Optical fiber is already massively deployed in the core network, and for feeding HFC and VDSL street cabinets. The standard single-mode optical fiber used in these networks has a theoretical bandwidth-distance product of 0.1 THz-km [2]. The deployment of a fiber network to the homes can therefore provide a future-proof infrastructure capable of supporting virtually unlimited data rates to the end users. Compared to any other network technology, wired or wireless, fiber also offers by far the best performance in terms of attenuation and cross section. So replacing the existing copper wires with optical fiber is a logical next step, alleviating the 'last mile' [3] speed bottleneck between the subscriber and his high speed local area network and the high speed core/metro network. The most popular fiber access networks are passive optical networks (PONs) with a point-to-multipoint (P2MP) topology: a single fiber leaves the optical line termination (OLT) at the LE or head-end and splits into multiple fibers each connecting to an optical network unit (ONU) at or close to the subscriber site. With this P2MP connection operators can divide the access network costs over all the users of that particular OLT. The network is called passive because there are no optical amplifiers or any components that need a power supply connection in the network. This means there are no components that need maintenance, which improves network reliability.

Over time, different fiber access network technologies were standardized and deployed. The first generation of PONs was called APON/BPON. They were standardized between 1998 and 2001 [4–6] and are now commercially available especially in USA. BPON offers customers 155/622 Mbit/s downstream and 155 Mbit/s upstream. A BPON connects up to 32 customers via one or more stages of passive optical splitters and, to avoid collisions between the upstream data, a time division multiple access (TDMA) protocol is used. BPON has a maximum reach of 20 km between the OLT and the customer ONU. This first generation of PONs was followed by Institute of Electrical and Electronical Engineers (IEEE) GE-PON [7]

and International Telecommunications Union (ITU-T) GPON [8–10]. From the viewpoint of the implementation of a burst-mode receiver (BM-Rx), the main differences between the two are the overhead time and data encoding. This second generation of PONs offers up to 1.25/2.5 Gb/s downstream and 1.25 Gb/s upstream. As the physical layer remains the same as in BPON the infrastructure is fully compatible with the already deployed infrastructure.

With the advent of these gigabit-rate PONs and the continually increasing speed of processors and the data capacity of information carriers, again, new applications emerged like videoconferencing, video on demand and peer-to-peer downloading. However, the introduction of triple-play (providing telephone, internet and digital video services via only one connection and one provider) necessitates even higher data rates than offered by second generation PONs. This is what third generation PONs or Next Generation PON (XG-PON) will offer: 10 Gb/s downstream and 10 or 2.5 Gb/s upstream for ITU-T XG-PON and symmetric 10 Gb/s for IEEE 10GE-PON [11].

No optical networks can function without the necessary optical and electrical components. In the PON downstream, continuous data is broadcast to all end users and the users filter out all data intended for other users. For this application, existing continuous components used in the (continuous) core/metro network can be reused although cost reduction for the ONU equipment remains a considerable challenge. In the upstream direction on the other hand, a TDMA protocol is used to share the fiber capacity amongst users. The TDMA data transmission is bursty and a special 'burst-mode' laser transmitter (Tx) and optical receiver (Rx) are required. These are a lot more challenging to design and typically emerge later on the market than their continuous counterparts designed for the same data rate.

1.2 First and Second Generation PONs

Figure 1.1 shows the architecture of a PON. The OLT is connected to the core/metro network through optical fiber (not shown in the figure). The access side of the OLT is connected to up to 32 ONUs via one or more optical splitters. The ONUs can be located in single houses, appartment buildings, business buildings or in end cabinets of a copper distribution network. The different PON fiber terminations have all received separate names in the past grouped into fiber-to-the-x (FTTx), where x is substituted by the location of the end point. E.g. ending the PON in the street cabinet ONU(n) in Figure 1.1 is called fiber-to-the-curb (FTTC). The connection between fiber end-point and users is then provided over copper. Ending the fiber connection in a building (not a residential home) is called fiber-to-the-building (FTTB). When the ONU is at a residential home, it is called fiber-to-the-home (FTTH). Several papers have discussed the deployment and economical aspects of FTTx [12–14].

Figure 1.2 shows the upstream data arriving at the OLT. The packets or bursts have different amplitudes because of the different fiber length and fiber attenuation between each ONU and the OLT. Also, the passive splitter/combiner introduces different losses due to splitter non-uniformities. The time between bursts

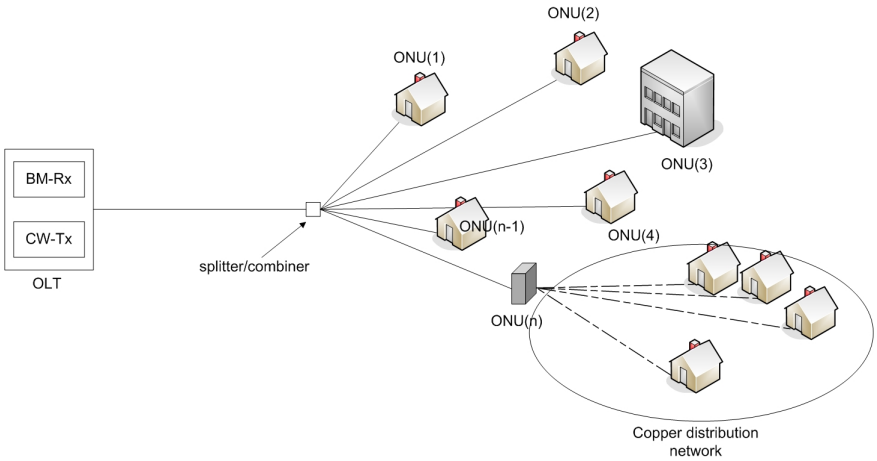

Figure 1.1: Passive optical network architecture - FTTx

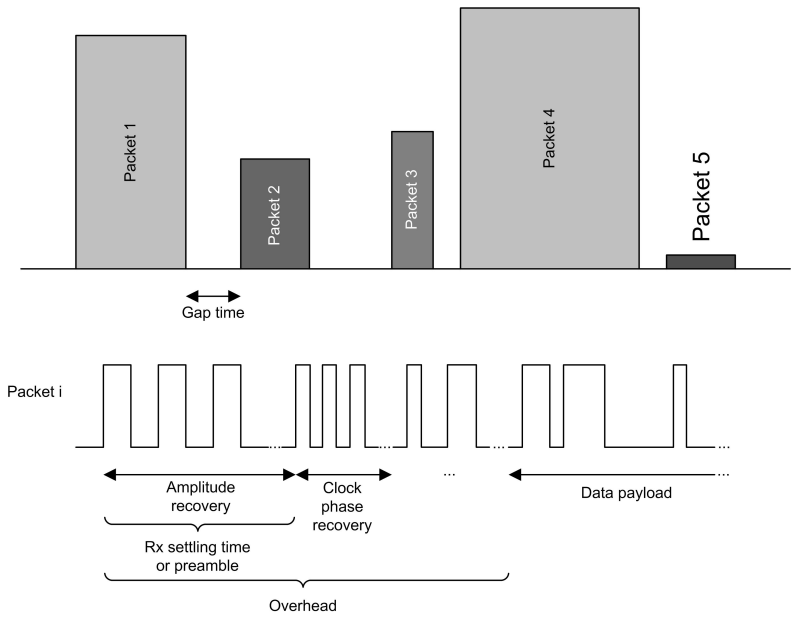

Figure 1.2: Upstream burst format in PON

is called the gap time or guard time and the minimum guard time is an important specification for the BM-Rx in the OLT. The lower part of Figure 1.2 shows one enlarged burst in the upstream direction. The data pattern at the beginning of the burst is the same for every packet and is called the preamble. It consists of a portion designed for the amplitude recovery and one for clock and phase recovery. The rest of the packet contains the data payload. The quick succesion of bursts with different amplitude is what makes the design of burst-mode (BM) electronics so challenging. Rx's that can cope with this kind of traffic are called BM-Rx's. They have to be able to recover correctly the data of all packets. Therefore, the BM-Rx detects amplitude and clock information during the preamble. During the guard time, the information of the previous burst must be erased and the Rx must prepare for the reception of the new bursts. It is clear that, the larger the difference between strong and weak bursts, and the shorter the guard times, the more difficult it will be to design a BM-Rx that can correctly receive all packets. For gigabit PONs two standards have been developed: IEEE GEPON and ITU-T GPON.

GEPONs use data encoding like 8B10B to dc-balance the transmitted data. This drastically decreases the network efficiency and therefore the achievable effective data rate goes down. As the data payload is dc-balanced ac-coupled Rx's can be used. This greatly simplifies the BM-Rx design.

In GPON the transmission efficiency is kept as high as possible. This means the shortest guard and preamble times, and no heavy coding on the data payload. The longest string of consecutive identical digits (CID) can be as long as 72 bits. The implication is that the data is not dc-balanced requiring a dc-coupled BM-Rx as the charge on the coupling capacitors of an ac-coupled BM-Rx would cause baseline wander [15] when used in GPON. The design reported in this dissertation concerns a dc-coupled GPON-like BM-Rx. The focus is also on the physical layer of the network and MAC-layer and protocols will therefore not be discussed.

1.3 Future Optical Networks

1.3.1 10 Gb/s optical networks

More and more applications require higher data transfer rates, and more and more data is being generated and shared (YouTube, Twitter, ...). The recent past has shown that future internet applications cannot be predicted. However, it is certain that even higher data rates will be required. This poses a lot of challenges both from telecom operator point of view and from the technical point of view. Telecom operators need to invest in the massive deployment of fiber, and in new equipment to send and receive the fast signals. The cost to deploy the network combined with the cost of keeping the network operational should not be much larger than the cost of the currently deployed networks, because customers are not prepared to pay

significantly more for a higher data rate. Also, investments for FTTx deployment should be returned from substitution of revenues (e.g. tripple play subscriptions pay for the past investments for broadband access) and it is foreseen that in Europe, a totally new architecture for optical networks is needed for these networks to be viable for the investing operators [16]. From a technical point of view, new and higher speed components are needed. At the starting time of this doctoral research, no 10 Gb/s BM-Rxs were commercially available. Two ways to move to 10 Gb/s PONs will be described in this section. The standardization for ITU-T XG-PON [11] started during and after the completion of the EU-funded FP6 IST 'Photonic Integrated Extended Metro and Access Network' (PIEMAN) project and this research work. The design of BM-Rx's for XG-PONs will be briefly introduced in Chapter 5.

1.3.2 High-split long reach optical PONs

GPON and GEPON are massively being deployed in many countries such as USA and Japan. However, Europe lags behind when it comes to deploying optical fiber. One explanation for this is given in [17] where it is shown that a rather uniform distribution of people requires a different concept of PONs than the traditional division between core network over long distances and the access network over a maximum of 20 km. A more flexible network approach with respect to maximum reach and maximum splitting factor would allow the optical networks to be used in much more diverse demographic situations, making the network more viable for European network operators than the currently commercialized network architectures. A first way to increase the reach and splitting factor is to use optical amplifiers. This was researched in the IST project PIEMAN (see section 1.4.2). Optical amplification will compensate for the large losses of longer fiber links and higher splitting factors. One drawback of these optically preamplified Rx's is the necessity of narrowband optical filtering which puts heavy requirements on the Tx in terms of wavelength stability. A second solution is to use avalanche photodiode (APD)s instead of PIN photodetector (PD)s. APDs have an intrinsic gain that can improve the sensitivity of the BM-Rx. If the maximum received power remains the same, then the ratio between maximum and minimum Rx optical power can be increased. As a consequence more flexibility concerning the geographical deployment of a fiber access network [18] is achieved. This is the subject of the Eu-funded FP7 ICT project 'Materials for Avalanche Receiver for ultImate SEnsitivity' (MARISE) (see section 1.4.3).

1.3.3 Next generation PONs

In the last couple of years the two standardizing bodies IEEE and Full Service Access Network (FSAN) have been working on standards for 10 Gb/s optical access

networks. The main idea is to reuse the existing GPON and GEPON infrastructure but upgrade the optoelectronic components to 10 Gb/s. As the infrastructure will be reused, the maximum split remains 32 and the maximum reach 20 km. An option is foreseen to increase the maximum reach to 60 km.

1.4 Overview of the Work

In the first years at INTEC_design I worked on the IWT project 'Fiber Optic Transceivers for Automotive Infotainment Networks' (AUTOFUN). For this project I designed an integrated PIN-TIA. Next I designed a burst-mode transimpedance amplifier (BM-TIA) and burst-mode post-amplifier (BM-PA) for the EU FP6 IST project PIEMAN. This PhD text discusses the work performed in this project. With the experience in TIA design I moved on to the EU FP7 ICT project MARISE, for which I have been designing a 10 Gb/s APD-TIA.

1.4.1 The IWT project AUTOFUN

In the IWT project AUTOFUN a 150 Mb/s non-return to zero (NRZ) Tx and 150 Mb/s NRZ Rx were designed. The design of the Tx chip was performed by my colleague Xin Yin [19, 20]. I designed the 150 Mb/s PIN-TIA chip. The partners in this project were:

- Melexis N.V.
- Melexis Tessenderlo N.V.
- imec (INTEC_design)

1.4.1.1 Optical networks in automotive

Recently, more and more sensors and also entertainment functions like DVD players are being introduced in cars. This leads to digital information that needs to travel over short distances within the car, typically less than 10 meters. Previously, all information was transmitted through copper wires, however, these have a number of disadvantages in the stringent environment of a car:

- Copper wires are very susceptible to electromagnetic interference (EMI). The electromagnetic fields in a car can range from 70 V/m till 200 V/m over the frequency range from 1 MHz till 3 GHz. Therefore, a large EMI immunity is required.
- The total weight of all the copper communication wiring adds to the weight of the car, increasing its fuel consumption.

For non-critical sensoring functions and low speed data communication, the EMI is not so critical. However, more and more critical car functions are also monitored by sensors. As the data is processed elsewhere in the car, this requires a very reliable data communication network. Optical fiber has the advantage of having a lower weight and it is also immune to EMI. Therefore, optical networks for automotive infotainment networks are a promising solution. Because of the low transmission distance, one can use large core fibers such as plastic optical fiber (POF) and plastic cladded silica (PCS) [21]. The larger core diameter simplifies fiber alignment, so that large-core connectors and transceivers can be made much cheaper than the ones used for monomode fiber connections. Lower component cost is an important requirement as a car can accomodate up to 100 optical transceivers. Besides the requirement of low-cost and EMI immunity, components within cars (application specific IC (ASIC)s and fiber itself) have to be able to withstand a temperature range from -40 °C up to 125 °C as the temperature in the hood of the car can raise significantly on a sunny summer's day.

The research performed within AUTOFUN was aimed at the development of flexible and reliable solutions to make innovative low-cost fiber optic Tx's and Rx's for automotive infotainment networks. The goal was to deliver the highest achievable optical budget at the lowest possible price. Innovative solutions were therefore required both in the field of packaging and assembly technology as well as in the field of opto-electronic Rx and Tx circuitry. To ensure a low-cost Rx solution, preferably the PD is integrated together with the Rx electronics onto the same die.

The advantages of monolithic integration of the PIN PD with the transimpedance amplifier (TIA) are:

- Low-cost (avoidance of an additional discrete component that otherwise needs to be mounted inside the Rx-module)
- Better EMI-immunity (avoidance of bond wire connections from the PD to the TIA input)
- Better control over PD dimensions.

However, a lot of disadvantages result from integrating a PD on a Si die for operation at a wavelength of 850 nm:

- Low responsivity of the Si PD at 850 nm, making high Rx sensitivity challenging.
- Carriers are generated deep into the Si substrate, giving rise to 'tails' in the impulse response of the PD. Such tails can potentially limit the bandwidth and Rx sensitivity

The transceiver was designed to anticipate the Media Oriented Systems Transport (MOST) standard [22] (which only started to emerge during the project).

1.4.1.2 Design of a BiCMOS TIA for automotive applications

Two test chips were designed during this project. The first test chip included the PIN PD, a TIA without automatic gain control and a post-amplifier (PA). The second test chip also included automatic gain control. The design was challenging as designing for the automotive environment poses extra challenges on the electronics:

- Automotive temperature range: Electronic circuits need to operate over an ambient temperature range of -40 °C to 125 °C.
- Cost-effectiveness: Automotive components need to be very low-cost. This implies the use of integrated PDs for the Rx front-end.

The aim of both test chips was to achieve the highest Rx sensitivity (better than - 24.5 dBm) at 150 Mb/s. Research was done to choose the best PD structure along with the front-end. Both chips were implemented in a 0.6μm BiCMOS technology with integrated PIN PD. The main challenges could be identified as:

- The large integrated PD with large capacitance reduces the achievable sensitivity and data rate.
- The large temperature range and large process spread: due to the low cost requirement only a simple trimming scheme can be used to trim away the process spread.

1.4.1.3 Results

The simulation results were published in [23]. The measurements of the first version performed at INTEC_design showed a sensitivity of - 27.7 dBm (average optical power) at an extinction ratio of 6 dB. At an extinction ratio of 10 dB the measured sensitivity was -29.1 dBm. The measured DC gain was 7.2 kΩ and the bandwidth was sufficient for 150 Mb/s NRZ transmission. Both Tx and Rx were also integrated in a 150 Mb/s demonstrator at Melexis. There it was shown that the sensitivity was -26 dBm and the overload was -16 dBm [24].

1.4.2 The FP6 IST Project PIEMAN

From 2006 to September 2008 I did research for the EU-funded FP6 IST project PIEMAN [25]. The partners in this project were

- Alcatel-Lucent
- Tyndall National Institute
- Centre for Integrated Photonics (CIP)

- imec (INTEC_design)
- British Telecom (BT)
- Nokia Siemens Networks (NSN)

Imec (INTEC_design) was responsible for designing 10 Gb/s BM-TIA and BM-PA chips. Initially, the INTEC_design was also responsible for designing a BM-Tx, but this task was completed with commercially available components, and therefore a 10 Gb/s BM-clock and data recovery (CDR) was also designed. Within PIEMAN I designed two versions of the 10 Gb/s BM-TIA and 10 Gb/s BM-PA prototypes.

1.4.2.1 10 Gb/s long reach optical networks with optical amplification

The research within PIEMAN focussed on the physical layer. The aim was to develop a radically new approach to optical networks [26–28]. The optical fiber network designed within PIEMAN can deliver access data rates of up to 10 Gb/s upstream and downstream to individual customers. At the same time it integrates access and metro networks into one system, thereby greatly simplifying the network architecture and so significantly reducing the cost to deliver future broadband services to residential and small and medium sized enterprises (SME) customers. An important novelty of the PIEMAN network was the introduction of dense WDM (DWDM) into the access network. For this, two Tx approaches were considered, a tunable 'Set-and-Forget'-laser which is set once to the appropriate wavelength and a reflective ONU-Tx whereby wavelength referencing is provided from the well-controlled environment of the central office.

Affordable bandwidth in the order of gigabits per second will offer new ways of working and more business opportunities for SMEs in Europe, thereby improving the employment and standard of living. One can only imagine the possibilities of a high bandwidth capacity for publishers, movie editors, engineers using computer aided design (CAD), scientists performing complex modeling at remote supercomputers, medical doctors assisting a surgery in a remote location, providers of high quality videos or games, branch offices connected to a corporate network via a high bandwidth virtual private network (VPN) connection, and other yet unknown applications. The tele-workers in Europe will benefit from the developments proposed in PIEMAN. Thanks to the increased access capacity to the premises of a business or SME, a server will be able to handle many connections to tele-workers that are logging in at home. The facilities for tele-working will reduce the time spent in traffic jams and increase the health and quality of life of European citizens. This will reduce the pollution and improve the safety in traffic.

1.4.2.2 Design of 10 Gb/s BM PIN-TIA and BM-PA chips

For PIEMAN I designed a 10 Gb/s dc-coupled BM-TIA and a 10 Gb/s dc-coupled BM-PA. An initial feasibility study revealed the following challenges:

- Modeling the interface between PD and BM-TIA
- Influence of module integration on performance of the TIA
- Combining high Rx sensitivity with large dynamic range
- Quickly switching and locking the gain setting of the TIA
- Removing the offset at the BM-PA within the preamble
- Minimizing BM penalty
- Reducing power consumption.

The specification of the BM-TIA at the beginning of the project were:

- BM Rx sensitivity of -16 dBm
- Overload of 0 dBm
- Total preamble (TIA + limiting amplifier (LA)) time of 128 ns
- Supply voltage of 2.5 V.

The specifications of the BM-PA at the beginning of the project were:

- Activity detection generation
- Total preamble time of 128 ns
- Threshold tracking to cope with erbium doped fiber amplifier (EDFA) gain transients
- BM penalty $<$4 dB
- CID tolerance $>$ 72 bits

PIEMAN targeted bit rates of 10 Gb/s upstream and downstream. At the start of this research, this had never before been attempted in a TDM PON. The state-of-the-art 10 Gb/s BM electronics in a PON at the start of the project was 1.25 Gb/s [29–32], so the aim of PIEMAN was to increase this data rate with a factor of 8.

The results from PIEMAN were published in several international journals [33–38] and conferences [27, 28, 38–43] and led to one patent application [44].

1.4.3 The FP7 ICT Project MARISE

From September 2008 until December 2009 I worked on the EU-funded FP7 ICT project MARISE [45]. The goal of the project was to design new materials for high-speed applications such as 10 Gb/s and 40 Gb/s BM-Rx's and quantum cryptography. The partners in MARISE are:

- Alcatel-Thales (III-V lab)
- IDQuantique
- The University of Sheffield
- Advanced Electro-optic Technologies (Adveotec)
- imec (INTEC_design)

Imec (INTEC_design) committed to design a 10 Gb/s and 40 Gb/s BM-TIA to prove the performance of the newly designed PDs in applications. I designed the 10 Gb/s APD-TIA. The challenging specifications are:

- High Rx sensitivity of -27 dBm
- Wide dynamic range of 21 dB
- APD gain and TIA gain switching on nanosecond scale.

To achieve this high sensitivity in combination with a large dynamic range, both the transimpedance gain and the avalanche gain are switched from burst to burst.

1.5 Overview of the thesis

The specific challenges burst-mode transmission poses on the design of Rx's for PONs are explained in Chapter 2. Also, some important figures of merit for the Rx are defined. The PIEMAN architecture is introduced and the BM-Rx specifications are summarized at the end of the chapter. Chapter 3 discusses the TIA design, from noise optimization to the circuits of the individual blocks on the TIA. The TIA's special features are explained and measurement results are shown. The BM-PA design is explained in Chapter 4. The different offset compensation mechanisms are introduced and the BM penalty is calculated. The special circuits and functions of the BM-PA are also explained. This chapter ends with the measurement results of the BM-Rx. Chapter 5 concludes this dissertation and suggestions for further research are given. The work performed for MARISE is also briefly touched.

References

[1] N.S. Bergano and C.R. Davidson. *Wavelength division multiplexing in long-haul transmission systems*. Journal of Lightwave Technology, 14(6):1299–1308, Jun. 1996.

[2] G.P. Agrawal. *Fiber-Optic Communication Systems*. John Wiley & Sons, 2002.

[3] P.E. Green. *Paving the last mile with glass - If US phone companies don't lay fiber, the cable industry will eat their lunch*. IEEE Spectrum, 39(12):13–14, Dec. 2002.

[4] ITU-T. *Recommendation G.983.1 - Broadband optical access systems based on Passive Optical Networks (PON)*, 1998.

[5] ITU-T. *Recommendation G.983.2 - ONT management and control interface specifications for ATM PON*, 2000.

[6] ITU-T. *Recommendation G.983.3 - A broadband optical access system with increased service capability by wavelength allocation*, 2001.

[7] *IEEE Standard 802.3ah Ethernet for the First Mile website*. `http://www.ieee802.org/3/efm/`.

[8] ITU-T. *Recommendation G.984.1 - Gigabit-capable Passive Optical Networks (G-PON): General Characteristics*, 2003.

[9] ITU-T. *Recommendation G.984.2 - Gigabit-capable Passive Optical Networks (G-PON): Physical Media Ddependent (PMD) layer specification*, 2003.

[10] ITU-T. *Recommendation G.984.3 - Gigabit-capable Passive Optical Networks (G-PON): Transmission convergence layer specification*, 2004.

[11] X.Z. Qiu, C. Mélange, T. De Ridder, B. Baekelandt, J. Bauwelinck, X. Yin, and J. Vandewege. *Evolution of burst mode receivers*. In 2009 35th European Conference on Optical Communication (ECOC), page 4 pp., Sept. 2009.

[12] M. Lafferty. *FTTx: an unreal reality takes shape*. CED, 28(3):32–4, 36, 38, Mar. 2002.

[13] K. Wieland. *FTTx roadblocks in Europe*. Telecommunications (International Edition), 40(6):18–20, 28, Jun. 2006.

[14] L. Hutcheson. *FTTx: Current status and the future*. IEEE Communications Magazine, 46(7):90–95, Jul. 2008.

[15] E. Rotem and D. Sadot. *Performance analysis of AC-coupled burst-mode receiver for fiber-optic burst switching networks*. IEEE Transactions on Communications, 53(5):899–904, May 2005.

[16] D.B. Payne and R.P. Davey. *The future of fibre access systems?* BT Technology Journal, 20(4):104–114, Oct. 2002.

[17] R. Davey, D. Payne, and A. Lord. *Optical networks: a pragmatic European operator's view*. In Optical Fiber Communications Conference. (OFC). Postconference Technical Digest (IEEE Cat. No.02CH37339), number vol.1, pages 41–2 vol.1, Mar. 2002.

[18] P. Ossieur, X.Z. Qiu, and J. Vandewege. *Analysis of optimum avalanche gain of burst-mode receivers for PON applications*. IEEE Photonics Technology Letters, 17(4):884–886, Apr. 2005.

[19] X. Yin, P. Ossieur, T. De Ridder, J. Bauwelinck, X.-Z. Qiu, and J. Vandewege. *An improved current-mode squarer/divider circuit for automotive applications*. IEICE Transactions on Electronics, E91C(2):232–234, Feb. 2008.

[20] X. Yin. *Het ontwerp van kosteffectieve en hoogperformante optische zenders voor gebruik in voertuigen*. PhD thesis, Dec. 2008.

[21] T. Wipiejewski, F. Ho, B. Lui, W. Hung, F.W. Tong, T. Choi, S.K. Yau, G. Egnisaban, T. Mangente, A. Ng, E. Cheung, and S. Cheng. *High performance fiber optic transceivers for infotainment networks in automobiles*. In Valldorf, J. and Gessner, W., editor, Advanced Microsystems for Automotive Applications 2005, pages 381–398, 2005. 9th International Forum on Advanced Microsystems for Automotive Application, Berlin, Germany, Mar. 16-18, 2005.

[22] *MOST Cooperation*. `http://www.mostcooperation.com`.

[23] T. De Ridder, P. Ossieur, X. Yin, B. Baekelandt, C. Mélange, J. Bauwelinck, X. Z. Qiu, and J. Vandewege. *BiCMOS variable gain transimpedance amplifier for automotive applications*. Electronics Letters, 44(4):287–288, Feb. 14 2008.

[24] O. Chasles. *150 Mbps demonstrator summary measurements report*. Melexis internal report.

[25] *PIEMAN project website*. `http://www.ist-pieman.org`.

[26] H. Rohde and S. Randel. *Project PIEMAN: A European approach to a symmetrical 10 Gbit/s, 100 km, 32 lambda and 512 split PON*. In Optical Transmission, Switching, and Subsystems IV, Pts 1 and 2, volume 6353 of *Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE)*,

pages U38–U45, 2006. Conference on Optical Transmission, Switching, and Subsystems IV, Gwangju, South Korea, Sept. 05-07, 2006.

[27] T. Davey, R. De Ridder, X.-Z. Qiu, P. Ossieur, H.-G. Krimmel, D. Smith, I. Lealman, A. Poustie, G. Talli, Chow C.W., P. Townsend, S. Randel, and H. Rohde. *Progress in IST project PIEMAN towards a 10 Gbit/s, multiwavelength long reach PON*. In Broadband Europe 2006, Geneva, Switzerland, Dec. 2006.

[28] X.Z. Qiu, Y.C. Yi, P. Ossieur, S. Verschuere, D. Verhulst, B. De Mulder, W. Chen, J. Bauwelinck, T. De Ridder, B. Baekelandt, C. Mélange, and J. Vandewege. *High performance burst-mode upstream transmission for next generation PONs*. In 2006 Asian Optical Fiber Communication & Optoelectronic Exposition and Conference (IEEE Cat No. 06EX1532), page 3 pp., 2006.

[29] M. Nakamura, Y. Imai, Y. Umeda, J. Endo, and Y.J. Akatsu. *1.25-Gb/s burst-mode receiver ICs with quick response for PON systems*. IEEE Journal of Solid-State Circuits, 40(12):2680–2688, Dec. 2005. IEEE International Solid-State Circuits Conference (ISSCC 2005), San Francisco, CA, Feb. 06-10, 2005.

[30] Q. Le, S.G. Lee, Y.H. Oh, H.Y. Kang, and T.H. Yoo. *A burst-mode receiver for 1.25-Gb/s ethernet PON with AGC and internally created reset signal*. IEEE Journal of Solid-State Circuits, 39(12):2379–2388, Dec. 2004. IEEE International Solid-State Circuits Conference (ISSCC 2004), San Francisco, CA, Feb., 2004.

[31] P. Ossieur, T. De Ridder, J. Bauwelinck, E. De Backer, J. Gillis, X. Z. Qiu, and J. Vandewege. *1.25 Gbit/s ITU-T G.984.2 burst-mode transimpedance amplifier without reset pins*. Electronics Letters, 43(18):991–993, Aug. 31 2007.

[32] P. Ossieur, D. Verhulst, Y. Martens, W. Chen, J. Bauwelinck, X.Z. Qiu, and J. Vandewege. *A 1.25-Gb/s burst-mode receiver for GPON applications*. IEEE Journal of Solid-State Circuits, 40(5):1180–1189, May 2005.

[33] B. Baekelandt, C. Mélange, J. Bauwelinck, P. Ossieur, T. De Ridder, X.Z. Qiu, and J. Vandewege. *OSNR penalty imposed by linear in-band crosstalk caused by interburst residual power in multipoint-to-point networks*. IEEE Photonics Technology Letters, 20(5-8):587–589, Mar.-Apr. 2008.

[34] P. Ossieur, C. Mélange, T. De Ridder, J. Bauwelinck, B. Baekelandt, X.Z. Qiu, and J. Vandewege. *Burst-Mode Electronic Equalization for 10-Gb/s*

Passive Optical Networks. IEEE Photonics Technology Letters, 20(17-20):1706–1708, Sept.-Oct. 2008.

[35] T. De Ridder, P. Ossieur, C. Mélange, B. Baekelandt, J. Bauwelinck, X. Z. Qiu, and J. Vandewege. *10 Gbit/s burst-mode post-amplifier with automatic reset*. Electronics Letters, 44(23):1371+, Nov. 6 2008.

[36] B. Baekelandt, C. Mélange, J. Bauwelinck, P. Ossieur, T. De Ridder, X.Z. Qiu, J. Vandewege, and G. Talli. *Polarization Dependence of Linear In-Band Crosstalk in Multipoint-to-Point Networks*. IEEE Photonics Technology Letters, 21(6):398–400, Mar. 15 2009.

[37] C. Mélange, B. Baekelandt, P. Demuytere, J. Bauwelinck, K. Van Renterghem, T. De Ridder, X. Z. Qiu, and J. Vandewege. *Mixed analogue/digital phase picking algorithm in oversampling burst-mode clock phase alignment*. Electronics Letters, 45(13):694–695, Jun. 18 2009.

[38] C. Mélange, B. Baekelandt, J. Bauwelinck, P. Ossieur, T. De Ridder, X.Z. Qiu, and J. Vandewege. *Burst-Mode CDR Performance in Long-Reach High-Split Passive Optical Networks*. Journal of Lightwave Technology, 27(17):3837–3844, Sept. 1 2009.

[39] T. De Ridder, P. Ossieur, B. Baekelandt, C. Mélange, J. Bauwelinck, C. Ford, Xing-Zhi Qiu, and J. Vandewege. *A 2.7 V 9.8 Gb/s burst-mode TIA with fast automatic gain locking and coarse threshold extraction*. In 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 220–1, 2008 2008.

[40] P. Ossieur, T. De Ridder, J. Bauwelinck, C. Mélange, B. Baekelandt, Xing-Zhi Qiu, J. Vandewege, G. Talli, C. Antony, P. Townsend, and C. Ford. *A 10 Gb/s burst-mode receiver with automatic reset generation and burst detection for extended reach PONs*. In 2009 Conference on Optical Fiber Communication - OFC 2009, page 3 pp., Piscataway, NJ, USA, Mar. 2009. IEEE. 2009 Conference on Optical Fiber Communication - OFC 2009, 22-26 Mar. 2009, San Diego, CA, USA.

[41] P. D. Townsend, G. Talli, C. W. Chow, E. M. MacHale, C. Antony, R. Davey, T. De Ridder, X. Z. Qiu, P. Ossieur, H. G. Krimmel, D. W. Smith, I. Lealman, A. Poustie, S. Randel, and H. Rohde. *Long reach passive optical networks*. In 2007 IEEE LEOS ANNUAL MEETING CONFERENCE PROCEEDINGS, VOLS 1 AND 2, IEEE Lasers and Electro-Optics Society (LEOS) Annual Meeting, pages 868–869, 2007. 20th Annual Meeting of the IEEE-Lasers-and-Electro-Optics-Society, Lake Buena Vista, FL, Oct. 21-25, 2007.

[42] S. Smolorz, H. Rohde, P. Ossieur, C. Antony, P.D. Townsend, T. De Ridder, B. Baekelandt, X.Z. Qiu, S. Appathurai, H.G. Krimmel, D. Smith, and A. Poustie. *Next generation access networks: PIEMAN and beyond*. 2009. International Conference on Photonics in Switching 2009 Pisa, Italy, Sept. 15-19, 2009.

[43] H.G. Krimmel, T. Pfeiffer, B. Deppisch, and L. Jentsch. *Hybrid electro-optical feedback gain-stabilized EDFAs for long-reach wavelength-multiplexed passive optical networks*. In 2009 35th European Conference on Optical Communication (ECOC), page 2 pp., Sept. 2009.

[44] B. Baekelandt, J. Bauwelinck, T. De Ridder, Ossieur P. Mélange, C., X.-Z. Qiu, and J. Vandewege. *Device and method for signal detection in a TDMA network*, May 2009.

[45] *MARISE project website*. `http://www.ict-marise.eu`.

2

Burst-Mode Receivers: Introduction

This chapter introduces some important BM-Rx concepts. These concepts illustrate the difficulties of the specific BM-Rx design. The PIEMAN optical network is explained in Section 2.2. Next, in Section 2.3 the imperfections of optical networks are discussed. These make the Rx design even more challenging. This chapter ends with Section 2.4, where the PIEMAN network specifications and the resulting BM-Rx specifications will be given.

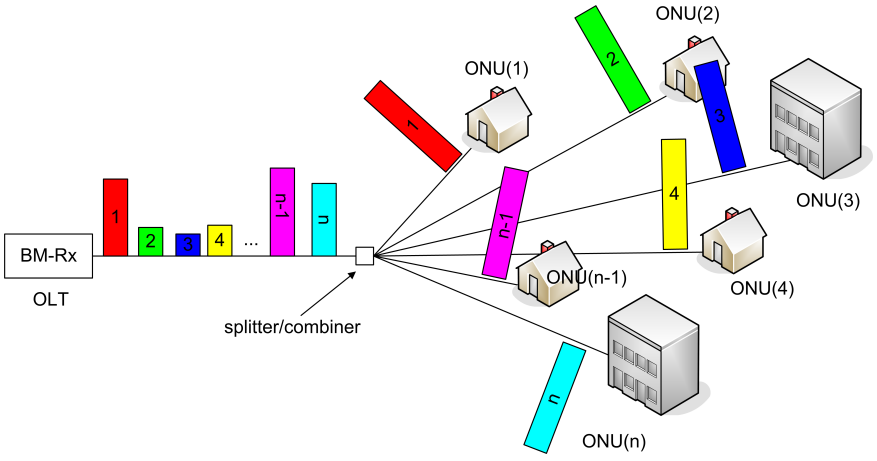

Figure 2.1: Basic PON operation - details of upstream transmission

2.1 Burst-Mode Receiver Concepts

2.1.1 Introduction

Figure 2.1 shows a general PON architecture with details of the upstream burst transmission. Several ONUs, which can be a customer's premises, a connection to the existing copper distribution network, or an appartment building, etc. are connected by optical fiber to an optical combiner/splitter. The combiner aggregates the signals from all ONUs onto one fiber in the upstream direction. In the downstream this combiner works as a splitter. This splitter is also connected to the OLT which is in turn connected to the core/metro network. The part between OLT and ONUs is called the optical distribution network (ODN).

In the downstream, the transmission protocol is rather simple. The Tx in the OLT sends out a continuous stream of packets intended for different ONUs. Every ONU receives this stream. Information at the beginning of each packet indicates the addressed ONU so an ONU can discard packets not intended for itself. As explained in Section 1.2, in the upstream, the packets sent by each ONU undergo a certain attenuation over the fiber between the respective ONU and the combiner. To avoid collisions of packets after the combiner, a strict timing protocol is needed. This protocol is called TDMA. It means that the OLT assigns a time slot to each ONU. The Tx's in the ONUs are only allowed to send out a packet in their assigned time slot. So, when the TDMA protocol is strictly followed the BM-Rx at the OLT will receive a sequence of packets, separated by a small time gap, and every packet will have a different strength due to the aforementioned splitter/fiber attenuation in the ODN.

In the core of each connection network, signals to be transmitted are dc balanced through coding and every packet has similar amplitude and phase. There are also no significant gaps in between packets. Traditional continuous-mode receiver (CW-Rx)'s can be used in those networks. These Rx's use ac-coupling for high Rx sensitivity. Slow measurements (or averaging) on the '0' and '1' levels of incoming signals yield an accurate decision threshold because the strength of the packet only varies slowly over time. The coding ensures sufficient transitions within long packets so a conventional continuous-mode CDR (CW-CDR) for precision clock phase acquisition can be used. Moreover, a slow automatic control loop (AGC) that yields a large dynamic range is possible. This dynamic range is the difference between the weakest and largest power a Rx can detect correctly. All these advantageous conditions and methods make it relatively easy to achieve high sensitivity and a wide dynamic range for CW-Rx's.

An OLT-Rx in conventional PONs receives optical packets from all active subscribers in fast succession, with varying signal level and phase from packet to packet. This is a totally different situation than in continuous wave (CW) networks and this quick succession of short packets with different amplitude and

phase puts very stringent requirements on the BM-Rx's at the OLT. A CW-Rx with ac-coupling and slow AGC function cannot react sufficiently fast to the quick change in optical input power that occurs from packet to packet. This results in packet loss due to baseline wander [1]. So, a CW-Rx is not suitable in this network architecture and BM-Rx's especially designed to cope with the burst traffic are required. Ac-coupling and a slow AGC function can still be used in BM-Rx's when combined with appropriate data encoding to ensure sufficiently dc-balanced signals, but only with a long guard time and preamble time. For short guard and preamble times in the order of a few tens of nanoseconds, dc-coupled BM-Rx's are required. In this case, little time is available to remove all memory (e.g. charge on a capacitor) of a preceding packet and to extract the decision threshold as well as to determine the sampling moment. The fact that all these things should happen almost instantaneously at the beginning of each burst leads to a significant sensitivity penalty, called BM penalty, which will be explained in Section 2.1.5. It also complicates the design of a very sensitive dc-coupled BM-Rx's with large dynamic range. Traditionally, two types of PONs have been explored. PONs based on the Ethernet protocol which use encoding to provide individually dc-balanced packets, called GE-PON. These PONs have been standardized by IEEE [2]. Due to the 8B10B encoding, ac-coupling can be used with little penalty and these types of BM-Rx's are called ac-coupled BM-Rx's [3, 4]. The other type of PONs driven by FSAN study group and standardized by ITU-T [5] focusses on the highest network efficiency, so heavy coding and large overhead are avoided. This means that guard and preamble times can become as short as 25.6 ns and 38.4 ns respectively for GPON. For this, ac-coupled BM-Rx's would incur a too large BM penalty, so special dc-coupled BM-Rx's should be used [6]. These are the most challenging to design from all three types of Rx's (CW-Rx's, ac-coupled BM-Rx's and dc-coupled BM-Rx's).

Figure 2.2 shows two elements of the BM-Rx and the BM-CDR with the processed signals. The optical signal P_{in} is converted into an electrical current by the opto-electric converter, mostly a PIN PD or an APD. This current is then amplified and converted into a voltage by the BM-TIA. The output of this TIA (V_1) is not yet compatible with logical levels. As shown in the figure, the signals can still contain different dc-offsets and different amplitudes from burst to burst. V_{th1} and V_{th2} are the ideal data decision levels of burst 1 respectively burst 2. Obviously, V_{th1} cannot be used as decision level for burst 2. So, offsets can impact on the data decision process, and therefore the BM-PA's job is to remove this offset and amplify the signals to logical levels, while performing the data decision based on an extracted threshold level. The data output by the post amplifier (V_2) is not aligned to the system clock in the OLT nor is the phase of both bursts the same. Therefore, the CDR or CPA extracts the clock phase (or sometimes also the clock) from the incoming burst. Now, the output of the BM-CDR is a sequence of equally

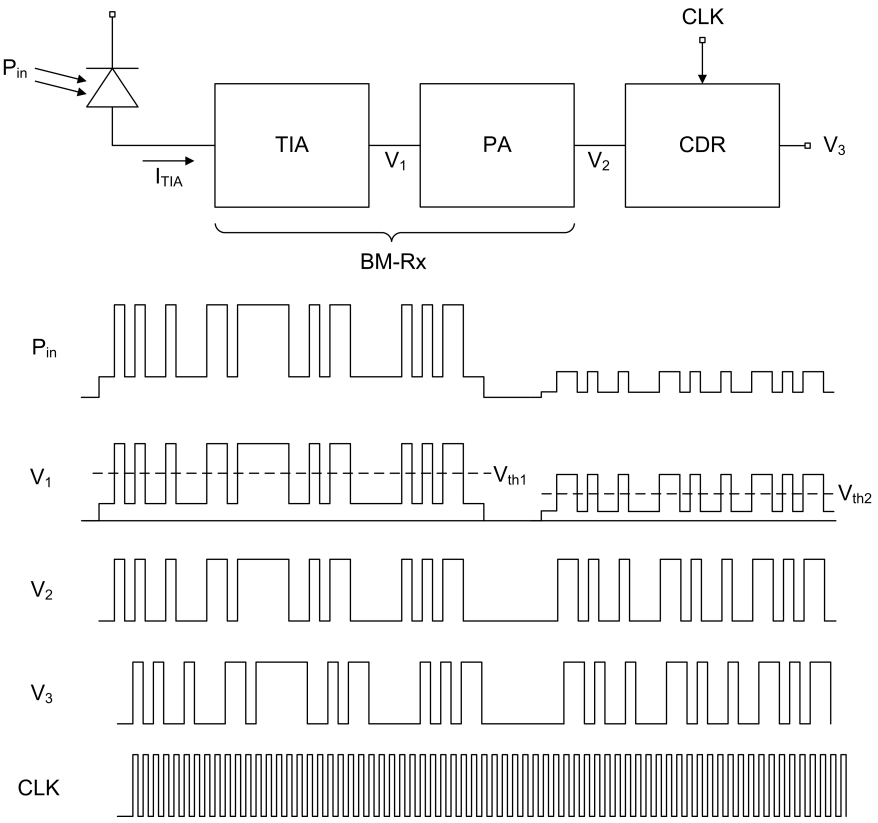

Figure 2.2: BM-Rx and BM-CDR signals

strong bits (V_3). This dissertation focusses on the design of a 10 Gb/s dc-coupled BM-TIA and BM-PA. The difficulties of the BM-CDR design will therefore not be covered in this PhD dissertation.

2.1.2 Automatic gain control

As can be seen from Figure 2.1 the weakest packet originates from the ONU that is located the furthest from the splitter. This packet will undergo the most attenuation. The strongest packet on the other hand has been sent by the ONU that is closest to the splitter. Both packets should still be received correctly by the BM-Rx.

The dynamic range (DR) of the BM-Rx is the ratio of maximum power that can be handled and mimimum power that can be detected by the BM-Rx. The DR determines the allowed maximum loss difference within the ODN. The sensitivity of the Rx, which is the optical power of the weakest burst that still can be detected

correctly by the BM-Rx, determines the maximum ODN loss. So it is clear that the geographical flexibility of a network highly depends on the performance of the BM-Rx and thus it is obvious that network operators prefer BM-Rx's with a combination of high sensitivity and large DR as this allows them to cover a large geographical area in a flexible manner.

The sensitivity of the BM-Rx in the absence of optical amplifiers is limited by the noise of the Rx and this in turn depends on semiconductor technology, chip architecture and/or a chosen opto-electrical converter [7–9]. To design a sensitive Rx, a large transimpedance gain (which is the gain between input current and output voltage of the TIA) is required. Unfortunately, the larger the transimpedance gain, the lower the Rx bandwidth, so the upper gain is limited [10]. On the other hand, to also allow the Rx to correctly detect very strong packets, a small transimpedance gain is wanted, as too large input currents will lead to distortion in the Rx. These very basic design rules show that there is a trade-off between Rx sensitivity and DR. An AGC system can help for this basic trade-off. In case of a continuously adjustable gain, the gain is typically modified by properly adjusting the gate voltage of a MOSFET by means of a feedback loop. This MOSFET is located in the feedback path and is used as a variable resistor [11]. If this should be done within a very short time frame it becomes extremely difficult to close the feedback loop in a stable manner. A feedforward solution can also be implemented. However, due to large process spread of the necessary MOSFETs it becomes very difficult to ensure the required pulse width distortion (PWD) over the entire DR. A better solution for dc-coupled BM-Rx's is to switch the gain as was done in [6, 12, 13], as this comes natural with the BM operation of the TIA. One then needs to quickly determine whether the burst amplitude is larger than a given reference, and to reduce the transimpedance gain if this is the case. The challenge at this point lies in doing this quickly and in ensuring that the gain remains in the same state throughout the complete burst.

2.1.3 DC offset compensation and threshold extraction

Figure (2.3) shows the BM-TIA output signals V_{outP} and V_{outN}. The total signal offset V_{os} can be defined as the difference between the threshold levels (V_{THP} and V_{THN}) of both phases. This offset should be removed. The offset can be divided into a burst dependent offset and a burst independent offset. The offset causes are explained next. Firstly, the outputs of the TIA will never be exactly equal to V_{cm} even when no optical power falls onto the PD, due to a small leakage current in the PD. This current is called the *dark current* and it is amplified along with any signal current present resulting in an unwanted output voltage shift. Secondly, tiny differences between identically dimensioned devices in the electronic circuits of the TIA will also give rise to an output voltage different to V_{cm}. To keep the

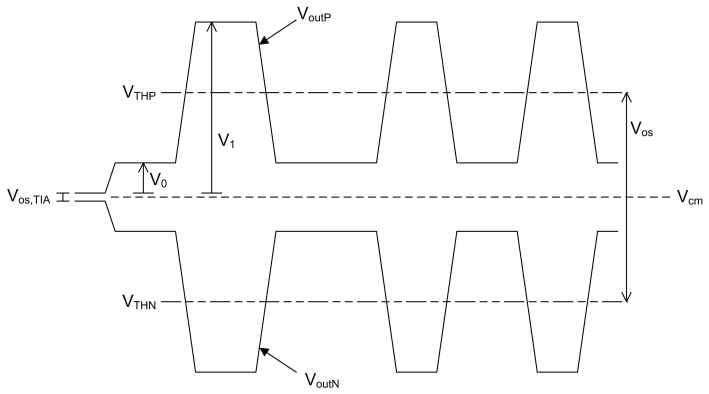

Figure 2.3: Offset at TIA output

drawing simple, these first two sources were combined into the differential offset $V_{os,TIA}$. The offset due to the mismatch between devices is stochastic, while the first offset cause is a deterministic cause. The resulting offset $V_{os,TIA}$ for a manufactured IC, however, is deterministic so it will be treated as a deterministic value in this section. Thirdly, the unipolar nature of the light makes that the positive signal phase V_{outP} is located above V_{cm} and the negative signal phase V_{outN} is located below V_{cm}. Lastly, the optical power for a zero will never be the ideal zero value. The power for a transmitted zero will always be a finite fraction of the power transmitted for a one. The ratio between the transmitted power for a one and the transmitted power for a zero is called the extinction ratio (ER). The TIA output signal can be written as (2.1) where V_{cm} is the ideal output level of the TIA, so without optical power incident on the PD and without internal sources of offset. b is the bit value (1 or 0).

$$V_{outP} = V_{cm} + \frac{V_{os,TIA}}{2} + (1-b)\,V_0 + bV_1, \quad b = 0,1 \tag{2.1}$$

$$V_{outN} = V_{cm} - \frac{V_{os,TIA}}{2} - (1-b)\,V_0 - bV_1, \quad b = 0,1 \tag{2.2}$$

From figure (2.3) it is clear that this offset is given by

$$V_{os} = V_{os,TIA} + V_0 + V_1 \tag{2.3}$$

For correct amplitude recovery, the offset V_{os} should be removed. The BM-PA will detect a threshold for the TIA output signal. This threshold is the voltage above which data is considered to be a '1' and below which data is interpreted as a '0'. This threshold should be chosen to minimize bit errors. Inaccurate measurements to determine this threshold will again cause offsets and these make the actual threshold differ from its ideal value leading to a BM penalty. From this

it is clear that offsets should be removed to optimize Rx performance. This can be done by extracting a threshold and amplifying against this threshold as this removes all signal offsets [14]. The amplifier itself (BM-PA) adds an extra offset however. Note that this amplifier offset is the same for every burst, it only depends on the device, temperature and supply and is therefore burst independent. This offset can only be removed through dc-offset compensation in the BM-PA while burst dependent offsets should be removed using threshold extraction.

In optical networks without optical amplifiers and without APDs the threshold that yields the least errors is located in the middle of the signal [10]. However, in case of APD noise or amplified spontaneous emission (ASE) noise, the optimum threshold is located slightly below the centre of the signal [15] because there is more noise on ones than on zeros.

2.1.4 Receiver sensitivity

The Rx sensitivity is defined as the minimum received power at the Rx needed to receive a data stream with a certain quality. This quality is mostly indicated by the number of bit errors averaged over the total number of received bits, the bit error ratio (BER). In the absence of noise and in an overly simplified view, one photon would be enough to correctly detect a '1' and no photon would be needed for a correct '0' reception. In reality, noise is always present, and more optical power is needed to detect a data stream with a certain BER than just one photon per bit.

Using a PIN PD (with responsivity R_{PD}) as opto-electrical converter, the current output I_S of this PD when an optical power P_{in} is received, is given by

$$I_S = R_{PD}P_{in} + i_n. \tag{2.4}$$

i_n is the noise present on the current in (2.4). This noise can be caused by the detector, the Rx itself or originate from optical noise [10, 16]. For simplicity it is first assumed that this noise is mainly caused by thermal noise present in the Rx. The BER P_e can be calculated from the noise probability distributions of the noise on '1' $p_1(x)dx$ and '0' $p_0(x)dx$ as the sum of the chance of detecting a '1' as a '0' and the chance of detecting a '0' as a '1'. In the simplest case, both '1' and '0' noise distributions are two equal normal distributions with respective averages and standard deviations $R_{PD}P_1$ and $R_{PD}P_0$, as well as σ_1 and σ_0 (P_1 and P_0 are the received optical power for a '1' respectively a '0'). Figure 2.4 illustrates this. As mentioned before, a threshold I_{DT} is needed to decide whether a received bit is either a '1' or a '0'. Every value above this threshold level is detected as a '1', every value below this threshold is detected as a '0'. As the aim is to minimize the BER, the threshold should be chosen to minimize the total error probability P_e. In the case of equal normal distributions, this optimized threshold is located at the cross-over point of both distributions which is halfway between '0' and '1'

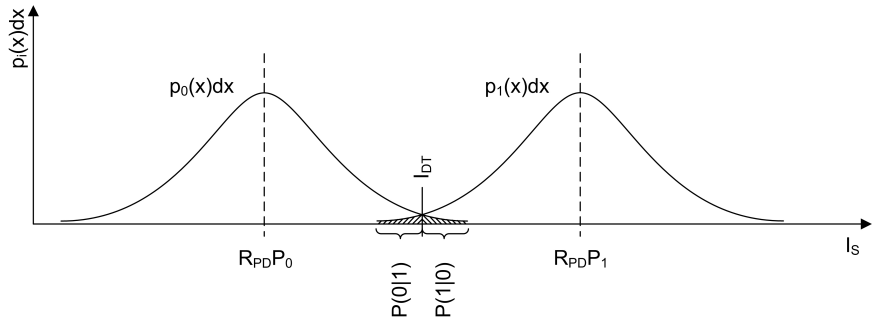

Figure 2.4: Noise distributions

average current levels [10]. The probability $P(1|0)$ that a '0' is wrongly detected as a '1' is equal to the area below the distribution from I_{DT} to infinity. This gives

$$P(1|0) = \int_{I_{DT}}^{\infty} p_0(x)\mathrm{d}x \tag{2.5}$$

$$= \frac{1}{\sqrt{2\pi}} \int_{Q}^{\infty} \exp\left(-\frac{u^2}{2}\right) \mathrm{d}u \tag{2.6}$$

where

$$Q = \frac{I_{DT} - R_{PD}P_0}{\sigma_0} \tag{2.7}$$

$$= \frac{i_{pp}}{2\sigma_0}. \tag{2.8}$$

In Equation (2.8) i_{pp} indicates the peak-to-peak current. As equal normal distributions were assumed, the probability of a bit error is given by

$$P_e = P(0) \cdot P\left(1|0\right) + P(1) \cdot P\left(0|1\right) \quad \text{with} \quad P(0) = P(1) = 0.5 \tag{2.9}$$

$$P_e = P(1|0) \quad \text{if} \quad P\left(1|0\right) = P\left(0|1\right) \tag{2.10}$$

$$= \frac{1}{2}\,\mathrm{erfc}\left(\frac{Q}{\sqrt{2}}\right). \tag{2.11}$$

From Equation (2.8) it is clear that Q, which is called the *Q-parameter* of *Personick* Q is a measure for the signal-to-noise ratio (SNR). Q can be calculated with (2.11) for every BER.

As will be shown in Section 2.3.1 there are noise mechanisms that cause a different distribution for the noise on the one and zero. In this case formula (2.10) is of course not valid and it should be replaced by the general form given by Equation

(2.9). In the end one can show [10] that P_e can be calculated by replacing (2.8) with

$$Q = \frac{i_{pp}}{\sigma_0 + \sigma_1}. \tag{2.12}$$

By explicitly writing the BER in function of the decision threshold I_{DT} and minimizing the BER using the threshold yields an expression for the ideal threshold level I_{DT} [16]

$$I_{DT} = \frac{\sigma_0 I_1 + \sigma_1 I_0}{\sigma_0 + \sigma_1}. \tag{2.13}$$

The minimum i_{pp} that yields a certain BER is called the electrical Rx sensitivity. This still has to be related to the optical Rx sensitivity (P_{sens}), which is the optical power averaged over time, that yields a certain BER. Assuming the input power for a zero is effectively zero (this requires a Tx with infinite ER) and neglecting the dark current, the average signal current $\bar{\imath}_S$ is given by $\frac{i_{pp}}{2}$. From (2.4) and (2.12) we get

$$\bar{P}_{sens} = \frac{i_{pp}}{2R_{PD}} \tag{2.14}$$

$$= \frac{Q\,(\sigma_0 + \sigma_1)}{2R_{PD}}. \tag{2.15}$$

In case of more than one uncorrelated Gaussian noise source, σ has to be calculated from the N individual σ's with [17]

$$\sigma = \sqrt{\sum_{k=1}^{N} \sigma_k^2}. \tag{2.16}$$

2.1.5 Burst-mode penalty

Several imperfections of the BM-Rx make that its sensitivity will be worse when receiving BM signals than a continuous mode Rx designed for the same speed. The difference between the two sensitivities is called the BM penalty. It can be understood from the fact that when imperfections such as offsets are present, one will need a higher optical input power to achieve the same Rx performance (BER). This extra power needed is the penalty and is expressed in dB. The need to quickly extract offset and phase of every burst also causes a BM penalty. This fast peak detection leads to a very noisy threshold [18–21]. The BM penalty is influenced by optical SNR (OSNR), dc level fluctuations, burst envelope distortion and chromatic dispersion. The BM penalty in the PIEMAN BM-Rx will be covered in more detail in Section 4.3.

2.2 PIEMAN Network Architecture

Traditionally, data networks have been divided in a metro part and an access part [22]. The metro part transports continuous data and therefore the cheaper and more advanced (higher speeds) continuous Tx's and Rx's can be used. The access part is the distribution network from local exchange to the customers like the one shown in Figure 2.1. In the downstream, continuous transmission is used. In the upstream the TDMA protocol is used, so BM-Tx's are needed at the ONU and BM-Rx's are needed at the OLT. As bandwidths grow, this traditional approach of separate access and metro networks will become prohibitively expensive:

- From capital expenditure (CAPEX) viewpoint due to the large number of network elements and interfaces to interconnect them
- From an operational expenditure (OPEX) viewpoint due to network design complexity, large number of network elements, large footprint and high electrical power consumption.

The PIEMAN project [23] proposed a radically different approach to photonic communication systems. The PIEMAN architecture integrates access and metro into one system. In order to achieve this for European national geographies it requires a reach of approximately 100 km from the customer to the major service node (SN). In such network there would typically be about 100 such major SNs in a typical European national network. This 100 km reach should enable full coverage and the option of dual parenting for resilience. Eventually every residential and SME customer will have fiber to the premises and in the PIEMAN architecture they will be directly and all-optically (i.e. no intervening optical-electrical-optical conversions) connected to a major SN up to 100 km away.

To deploy point-to-point (P2P) fiber from each customer to the SN located up to 100 km away would be prohibitively expensive. PIEMAN therefore uses multi-wavelength, high split PONs to make efficient use of fiber. PIEMAN performed physical layer research aimed at a third generation PON which will offer features totally beyond the capability of today's PONs. PIEMAN high level features are:

- Bandwidth per wavelength of 10 Gb/s downstream and 10 Gb/s upstream
- Each 10 Gb/s wavelength is shared by up to 512 customers
- Significant use of DWDM to provide further fiber efficiency: up to 32 wavelengths, each carrying 10 Gb/s. The project will therefore take a hybrid DWDM/TDMA approach
- All-optical reach of up to 100 km using EDFA's at the headend of the PON and at local exchanges. No use of optical-electrical-optical conversions at intermediate locations

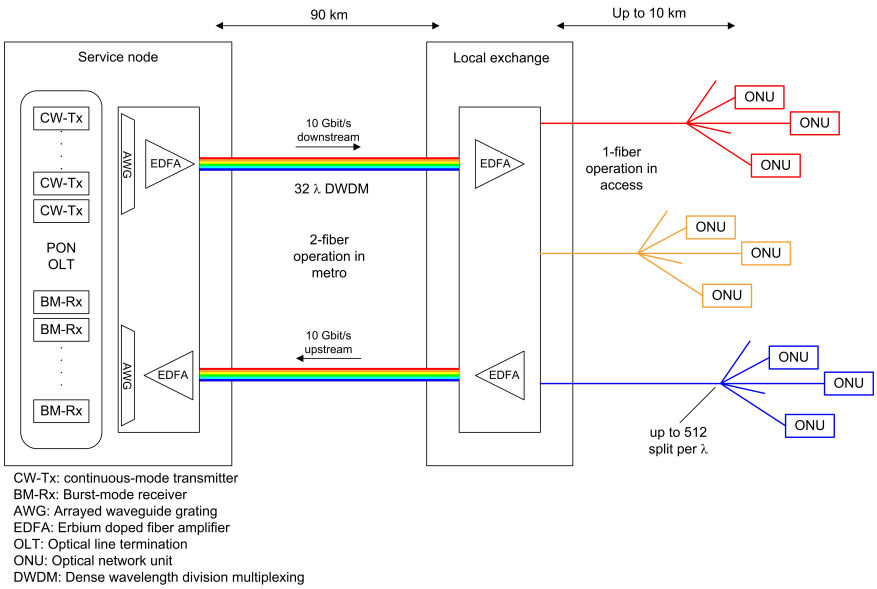

Figure 2.5: PIEMAN network architecture

- Single fiber connection to the customer.

The PIEMAN system architecture is shown in Figure 2.5. The OLT at the SN is connected to the LE over up to 90 km of metro fiber. In this section of the network, 2 fibers are used and their bandwidth is shared among 32 wavelengths using DWDM. At the LE, an arrayed waveguide (AWG) demultiplexes the 32 wavelengths onto 32 sub-PONs. Within these, passive splitters are used to branch out to the customer sites. Due to the high splitting factor of up to 512 and the long feeder section, amplification is necessary to compensate for the large losses. Dispersion compensating fiber (DCF) is included in the SN. This compensates for the dispersion of the 90 km fiber between LE and OLT. Note that the dispersion in the ODN cannot be compensated with DCF as each ONU is located at a different distance from the LE. In the 32 sub-PONs, the TDMA protocol is used in the upstream direction to accommodate up to 512 ONUs. This implies that the BM-Rx at the SN has to deal with a quick succession of packets with strongly varying optical power [24].

For the BM-EDFA in the local exchange, an active stabilization was developed by Alcatel-Lucent and tested within the PIEMAN project. Through the use of an auxiliary light source, gain peak excursions are minimized [25]. The critical case for system calculations is a low-power packet, for which 0.5 dB gain excursion was measured at the EDFA [26, 27]. Therefore the component of the BM penalty due to the BM-EDFA can be reduced to ~ 0.5 dB. EDFA gain excursions will therefore

not be considered in the design of the BM-PA.

2.3 Noise and Network Impairments

In Section 2.1 we considered an ideal network and mostly ideal Rx's and Tx's. In reality, a Tx never achieves an infinite ER, fiber is not an ideal transmission medium at high data rates and optical amplifiers introduce ASE noise. These network impairments will be briefly introduced in this section.

2.3.1 Photodetector noise

Not only the Rx produces noise, the PD itself also adds to the total noise and thus degrades sensitivity. A PIN PD produces shot noise alongside the signal current. The origin of this noise lies in the operation of PDs. When a photon is absorbed by the PIN PD, an electron-hole pair is created. However, this happens at a discrete time and thus the total signal current is made up from a number of discrete pulses spread over a certain time period. This means the signal current is a constant I_S but with noise on top (noise can be positive or negative). The shot-noise spectrum is white and its mean-square value $\bar{i}^2_{n,PIN}$ is given by [28]

$$\bar{i}^2_{n,PIN} = 2qI_{PIN}BW_n, \tag{2.17}$$

where BW_n is the bandwidth in which the noise current is measured, I_{PIN} is the PD current and q is the electron charge. As the noise current is signal dependent, the noise on a '1' will be larger than the noise on a '0'.

As mentioned in Section 2.1.3, every PD always produces a dark current, so shot noise will always be present even when no optical power is received. However, this dark current is mostly negligible compared to the signal current and therefore the shot noise generated by the dark current is usually neglected next to the signal-shot noise in noise calculations.

If the PD is an APD, avalanche noise is present. Like in the PIN, every photon generates an electron-hole pair. In an avalanche detector, every photon generates more than one electron-hole pair, with the number of electron-hole pairs a random value. The gain of the APD, called the *multiplication gain* or *avalanche gain*, is then equal to the average number of electron-hole pairs per absorbed photon. But similar to the PIN, one will get the signal current with a noise added on top. This noise is larger than just the shot noise current amplified by the multiplication gain. The mean-square noise current $\bar{i}^2_{n,APD}$ is given by Equation (2.18) [29].

$$\bar{i}^2_{n,APD} = FM^2 2qI_{PIN}BW_n \tag{2.18}$$

F is the excess noise factor and M is the avalanche gain. I_{PIN} is the primary PD current which is the current before avalanche multiplication. The excess noise

factor is given by Equation (2.19)

$$F = k_A M + (1 - k_A)\left(2 - \frac{1}{M}\right), \tag{2.19}$$

where k_A is the ratio of ionization coefficients of holes and electrons [28]. Increasing M enhances the signal, but also increases the noise. As the sensitivity is determined by the SNR there is an optimum avalanche gain that yields best Rx sensitivity. Equation (2.18) shows that the avalanche noise current also depends on the signal. So the noise on a '1' will again be larger than the noise on a '0'. An APD also has a primary dark current I_{DP} which is amplified along with the signal current. The noise current resulting from this dark current is given by substituting $I_{PIN} = I_{DP}$ in Equation (2.18). This noise current is mostly negligible.

To calculate the Rx sensitivity in case of a PIN of APD, one has to combine the standard deviations from thermal noise and shot noise, or thermal noise and avalanche noise as explained by (2.16).

2.3.2 Optical amplifier noise

Optical amplifiers, like semiconductor optical amplifiers (SOA)s and EDFAs, are used in the PIEMAN network to increase the output power of a Tx, to compensate for the losses in the network and as a preamplifier to increase Rx sensitivity. The noise introduced by the EDFA stems from ASE. The power spectral density (PSD) of this ASE noise can be modeled as white Gaussian noise with single sided spectral density S_{ASE} with [15]

$$S_{ASE} = N_{sp} h\nu (G - 1), \tag{2.20}$$

where N_{sp} is called the noise enhancement factor, G is the linear EDFA gain, h is the Planck constant and ν is the frequency. The optical noise power is given by

$$P_{ASE} = S_{ASE} BW_O. \tag{2.21}$$

As it is proportional to the optical filter bandwidth BW_O, the noise can be reduced by reducing the filter bandwidth. This is the noise in one polarization mode.

A PD converts the optical power linearly (2.22) to an output current. The device has a quadratic relation to the amplitude of the signal however. This causes the optical amplified noise to beat with the optical signal so the electrical field has to be considered.

$$I_{PD} = R_{PD} \cdot P_{in} \tag{2.22}$$

$$= R_{PD} \cdot |E(t)|^2 \tag{2.23}$$

The electrical field $E(t)$ at the input of the PD can be written as [30]

$$E(t) = \sqrt{G} s(t) \exp\left(j\phi_s(t)\right) + n_{ASE}(t) \tag{2.24}$$

with

$$n_{ASE}(t) = n_c(t) + jn_s(t) \tag{2.25}$$

The intensity incident on the PD is then given by

$$P(t) = E(t)E^*(t) = \left(\sqrt{G}s(t)\exp\left(j\phi_s(t)\right) + n_{ASE}(t)\right) \cdot \left(\sqrt{G}s(t)\exp\left(-j\phi_s(t)\right) + n^*_{ASE}(t)\right). \tag{2.26}$$

With Equation (2.25) this yields

$$\begin{aligned} P(t) &= Gs^2(t) + |n_{ASE}(t)|^2 \\ &\quad + 2\sqrt{G}s(t)\Re\left(n_{ASE}(t)\exp\left(-j\phi_s(t)\right)\right) \qquad (2.27) \\ &= Gs^2(t) + \left[n_c^2(t) + n_s^2(t)\right] \\ &\quad + 2\sqrt{G}s(t)\left[n_c(t)\cos(\phi_s(t)) + n_s(t)\sin(\phi_s(t))\right]. \qquad (2.28) \end{aligned}$$

The first term in (2.28) is the optical signal power which would also be present if there was no ASE noise. The second and third terms are the beat products of the ASE noise. The second term is the beat product between both quadrature components of the ASE noise itself and is called the ASE-ASE beat noise or spontaneous-spontaneous beat noise. The third component is called the signal-ASE (or signal-spontaneous) beat noise. These noise products will also give rise to a shot noise current. So in the electrical domain, there will not only be an extra noise term due to the ASE noise, there will also be extra shot noise terms. The PD output can be calculated from multiplying (2.28) with the PD responsivity R_{PD} and adding thermal and shot noise components. All these noise terms can be combined to one noise current with σ^2 given by Equation 2.29. [16]

$$\sigma^2 = \sigma_T^2 + \sigma_{sig,shot}^2 + \sigma_{sig,ASE}^2 + \sigma_{ASE,shot}^2 + \sigma_{ASE,ASE}^2 \tag{2.29}$$

σ_T^2 is the thermal noise of the Rx. The other terms are given by [31]

$$\begin{aligned} \sigma_{ASE,ASE}^2 &= 4R_{PD}^2 S_{ASE}^2 BW_o BW_e & (2.30) \\ \sigma_{ASE,shot}^2 &= 4R_{PD} q S_{ASE} BW_o BW_e & (2.31) \\ \sigma_{sig,ASE}^2 &= 4R_{PD}^2 G P_S S_{ASE} BW_e & (2.32) \\ \sigma_{sig,shot}^2 &= 2R_{PD} q G P_s BW_e. & (2.33) \end{aligned}$$

The factor 4 originates from the fact that S_{ASE} is the single-sided noise spectral density in only one polarization mode and so the number has to be doubled to account for the noise in both polarization modes in case there are no polarizers present in the optical network. Table 2.2 shows the ASE induced noise currents calculated using equations (2.30-2.33) with the parameter values in Table 2.1.

Parameter	Name	Value	Unit
Optical bandwidth	BW_o	0.1	nm
Electrical bandwidth	BW_e	7.5	GHz
Single-sided PSD (one polarization mode)	S_{ASE}	2.9e-17	W/Hz
Photodiode responsivity	R_{PD}	1	A/W
Wavelength	λ	1550	nm
EDFA Gain	G_1	39.3	dB
EDFA Gain	G_2	17	dB
EDFA noise figure	NF_1	5	dB
EDFA noise figure	NF_2	5	dB
Loss fiber	$Loss_1$	36.8	dB
Loss AWG	$Loss_2$	6	dB
Loss fiber	$Loss_3$	27	dB
Loss AWG	$Loss_4$	6	dB

Table 2.1: Parameters for calculating Table 2.2 values

Term (μA or μArms)	$B_o = 12.5$ **GHz (0.1 nm)**
Avg. current @ -16 dBm	25.12
Signal shot noise	0.24
ASE shot noise	0.04
ASE-signal beat noise	4.67
ASE-ASE beat noise	0.56
Typical thermal input referred noise	1.25

Table 2.2: ASE induced currents

These numbers are based on the average signal power. Equations (2.34,2.35) can be used to calculate the noise current on a '1' and '0' respectively.

$$I_1 = \frac{2I_{avg}}{1+ER} \tag{2.34}$$

$$I_0 = \frac{2ERI_{avg}}{1+ER} \tag{2.35}$$

where I_{avg} indicates the average photocurrent, I_1 and I_0 the photocurrent for a '1', '0' respectively. ER is the linear ER.

From this we can conclude that

- there is a large difference between the rms (root mean square) noise on the 1's and the rms noise on the 0's. The impact on the BM-PA is that it should

have a threshold placed lower than half the eye opening otherwise a sensitivity penalty will be incurred.

- the shot noise can be neglected compared to the thermal noise and the ASE-signal and ASE-ASE noise.

2.3.3 Chromatic dispersion

Different wavelengths have a different velocity in the fiber. This phenomenon is called chromatic dispersion. The spectrum of the transmitted signal has a certain bandwidth so the pulse is spread out over time. There are several ways to reduce the effect of dispersion, e.g.:

- Use narrow linewidth Tx
- Use wavelength around minimum dispersion window of fiber (1300 nm)
- Use dispersion compensating fiber to compensate for the dispersion
- Perform electrical dispersion compensation in the Rx [32–36].
- Use fibre gratings [16]

2.4 PIEMAN Physical Layer Upstream and BM-Rx Specifications

In an optical network without optical amplifiers, the BM-Rx sensitivity and maximum output power of the Tx determine the maximum link loss. When amplifiers are present the amplifier noise can cause a low OSNR. The achievable OSNR must exceed the required OSNR in order to guarantee the specified target BER. When the OSNR becomes too low the Rx will no longer be able to detect the burst correctly regardless of its own sensitivity. A network is called OSNR limited when the OSNR determines the optical power budget. The PIEMAN network is an example of such a network. The mean launched power (min. and max. P_{out0}) of an ONU, and the sensitivity as well as the overload capability of the OLT BM-Rx must guarantee correct operation over the range of the worst case access loss (10 km and 512 split) and the metro loss. The upstream optical power budget is determined by the achievable OSNR at the OLT BM-Rx. Several factors increase the total OSNR requirement such as the BM penalty and chromatic dispersion, while the use of forward error correction (FEC) provides an estimated coding gain of 5 dB [26]. For the BM-Rx design it was assumed that a sufficient OSNR of 22.5 dB was achieved in front of the OLT BM-Rx, as required for BER=10^{-10}.

The BM-Rx input level was specified as -13 dBm. Due to the fact that the PIEMAN LR-PON system is OSNR limited, the min. (sensitivity) and max. (overload) input mean optical level of the OLT BM-Rx can be adjusted (not independently) by a preamplifier EDFA. However, the maximum input mean optical level in front of the BM-Rx will be restricted by the maximum allowed optical power that can be launched onto a 10G PIN PD. This strongly depends on the maximum reverse current the PIN PD can handle. The PIN PDs could be damaged by overheating caused by continuous optical overload (or exceeding the maximum reverse current) on a millisecond time scale. In a network where the TDMA protocol is applied the optical overload will be bursty so overload conditions will only last for a short duration of time e.g. on a microsecond time scale so it is unlikely to be damaged. The chosen 10 G PIN PD can safely and linearly handle $<$ 3 dBm average optical power. On the other hand the overload level of the BM-Rx will also be limited by the electronics design of the BM-TIA and the BM-PA. It is not easy to handle such a big input current (0 dBm optical power means 1 mA input current) at the BM-TIA input. Therefore the overload specification was put at 0 dBm. Given the required 15 dB DR this results in a Rx sensitivity of -15 dBm. Even though the PIEMAN network is OSNR limited, the BM-TIA will be optimized for highest sensitivity in Chapter 3 and ASE noise will be neglected in the design. This allows the BM-TIA to be used in more general applications.

The bit rate was specified at 10 Gb/s with a fallback option of 5 Gb/s. This allowed to also demonstrate the feasibility of the network even if some components would not achieve their bandwidth specification. The data will be scrambled and transmitted in NRZ format. The BM-Rx has to deal with the worst case ONU Tx ER of 10 dB. The total preamble length was set at 30.4 ns of which 26.4 ns can be used for the BM-TIA and BM-PA. The rest is reserved for the clock phase recovery in the BM-CDR. The BM-Rx has to prepare for a new burst within 25.6 ns and has to cope with a sequence of at least 72 CID.

The top-level specifications of the 10 Gb/s BM-Rx are summarized in Table 2.3.

Items	**Unit**	**Specification**	**Remark**
Bit rate	Gb/s	10	Fall-back: 5 Gb/s
Wavelength	nm	1530-1542.8	
Line code		Scrambled NRZ	
Operation mode		Burst-mode	
ONU ER	dB	≥ 10	
Min. Rx Sensitivity	dBm	-15	less than 10^{-10} (OSNR = 22.5dB/0.1nm)
Min. overload	dBm	0	with optical preamplification
Rx dynamic range	dB	15	with $\pm$ 15 % PWD
Consecutive identical digits immunity	bit	> 72	
Preamble length	ns	30.4	33 (Rx) + 5 (CDR) = 38 bytes (PA)
Guard time	ns	25.6	32 bytes = 256 bits

Table 2.3: Key parameters and specifications of the PIEMAN 10 Gb/s BM-Rx

References

[1] E. Rotem and D. Sadot. *Performance analysis of AC-coupled burst-mode receiver for fiber-optic burst switching networks*. IEEE Transactions on Communications, 53(5):899–904, May 2005.

[2] *IEEE Standard 802.3ah Ethernet for the First Mile website*. `http://www.ieee802.org/3/efm/`.

[3] Q. Le, S.G. Lee, Y.H. Oh, H.Y. Kang, and T.H. Yoo. *A burst-mode receiver for 1.25-Gb/s ethernet PON with AGC and internally created reset signal*. IEEE Journal of Solid-State Circuits, 39(12):2379–2388, Dec. 2004. IEEE International Solid-State Circuits Conference (ISSCC 2004), San Francisco, CA, Feb., 2004.

[4] Q. Le, S.G. Lee, H.Y. Kang, and S.H. Chang. *A CMOS Burst-Mode TIA with Step AGC and Selective Internally Created Reset for 1.25Gb/s EPON*. In 2007 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 50–51, Feb. 2007.

[5] *Gigabit-capable Passive Optical Networks (GPON): Physical Media Dependent (PMD) layer specification*. ITU-T Recommendation G.984.2.

[6] P. Ossieur, D. Verhulst, Y. Martens, W. Chen, J. Bauwelinck, X.Z. Qiu, and J. Vandewege. *A 1.25-Gb/s burst-mode receiver for GPON applications*. IEEE Journal of Solid-State Circuits, 40(5):1180–1189, May 2005.

[7] S.D. Personick. *Receiver Design for Optical Fiber Systems*. Proceedings of the IEEE, 65(12):1670–1678, 1977.

[8] S.D. Personick, P. Balaban, J.H. Bobsin, and P.R. Kumar. *Detailed Comparison of 4 Approaches to Calculation of Sensitivity of Optical Fiber System Receivers*. IEEE Transactions on Communications, 25(5):541–548, 1977.

[9] T. Vanisri and C. Toumazou. *Integrated High-Frequency Low-Noise Current-Mode Optical Transimpedance Preamplifiers - Theory and Practice*. IEEE Journal of Solid-State Circuits, 30(6):677–685, Jun. 1995.

[10] E. Säckinger. *Broadband Circuits for Optical Communication*. John Wiley & Sons, 2005.

[11] T. De Ridder, P. Ossieur, X. Yin, B. Baekelandt, C. Mélange, J. Bauwelinck, X. Z. Qiu, and J. Vandewege. *BiCMOS variable gain transimpedance amplifier for automotive applications*. Electronics Letters, 44(4):287–288, Feb. 14 2008.

[12] M. Nakamura, Y. Imai, Y. Umeda, J. Endo, and Y.J. Akatsu. *1.25-Gb/s burst-mode receiver ICs with quick response for PON systems*. IEEE Journal of Solid-State Circuits, 40(12):2680–2688, Dec. 2005. IEEE International Solid-State Circuits Conference (ISSCC 2005), San Francisco, CA, Feb. 06-10, 2005.

[13] P. Ossieur, T. De Ridder, J. Bauwelinck, E. De Backer, J. Gillis, X. Z. Qiu, and J. Vandewege. *1.25 Gbit/s ITU-T G.984.2 burst-mode transimpedance amplifier without reset pins*. Electronics Letters, 43(18):991–993, Aug. 31 2007.

[14] P. Ossieur, T. De Ridder, X.Z. Qiu, and J. Vandewege. *Influence of random DC offsets on burst-mode receiver sensitivity*. Journal of Lightwave Technology, 24(3):1543–1550, Mar. 2006.

[15] P.A. Humblet and M. Azizoglu. *On the Bit Error Rate of Lightwave Systems with Optical Amplifiers*. Journal of Lightwave Technology, 9(11):1576–1582, Nov. 1991.

[16] G.P. Agrawal. *Fiber-Optic Communication Systems*. John Wiley & Sons, 2002.

[17] Luc Taerwe. *Waarschijnlijkheidsrekening en statistiek*. Cursus 2de kandidatuur burgerlijk ingenieur 2005-2006.

[18] C.A. Eldering. *Theoretical Determination of Sensitivity Penalty For Burst Mode Fiber Optic Receivers*. Journal of Lightwave Technology, 11(12):2145–2149, Dec. 1993.

[19] P. Menendez-Valdes. *Performance of Optical Direct Receivers Using Noise-Corrupted Decision Threshold*. Journal of Lightwave Technology, 13(11):2202–2214, Nov. 1995.

[20] M.S. Leeson. *Calculation of sensitivity penalty for optically preamplified burst mode receivers using Fabry-Perot filters*. Electronics Letters, 34(11):1121–1122, May 28 1998.

[21] P. Ossieur, X.Z. Qiu, J. Bauwelinck, and J. Vandewege. *Sensitivity penalty calculation for burst-mode receivers using avalanche photodiodes*. Journal of Lightwave Technology, 21(11):2565–2575, Nov. 2003.

[22] C. Lam. *Passive Optical Networks - Principles and Practice*. Elsevier, 2007.

[23] *PIEMAN project website*. `http://www.ist-pieman.org`.

[24] T. Davey, R. De Ridder, X.-Z. Qiu, P. Ossieur, H.-G. Krimmel, D. Smith, I. Lealman, A. Poustie, G. Talli, Chow C.W., P. Townsend, S. Randel, and H. Rohde. *Progress in IST project PIEMAN towards a 10 Gbit/s, multiwavelength long reach PON*. In Broadband Europe 2006, Geneva, Switzerland, Dec. 2006.

[25] H.G. Krimmel, T. Pfeiffer, B. Deppisch, and L. Jentsch. *Hybrid electro-optical feedback gain-stabilized EDFAs for long-reach wavelength-multiplexed passive optical networks*. In 2009 35th European Conference on Optical Communication (ECOC), page 2 pp., Sept. 2009.

[26] PIEMAN consortium. *D1.4 Addendum, Final PIEMAN system architecture, planning rules and business benefits. Update*. Technical report, August 2009.

[27] C. Antony, P. Ossieur, G. Talli, P.D. Townsend, H.G. Krimmel, A. Poustie, R. Wyatt, B. Harmon, I. Lealman, G. Maxwell, D. Rogers, and D.W. Smith. *Upstream burst-mode operation of a 100 km reach, 16 * 512 split hybrid DWDM-TDM PON using tuneable external cavity lasers at the ONU-side*. In 2009 35th European Conference on Optical Communication (ECOC), page 2 pp., Sept 2009.

[28] S.M. Sze. *Physics of semiconductor devices*. Wiley-Interscience, 1981.

[29] R.J. McIntyre. *Multiplication Noise in Uniform Avalanche Diodes*. IEEE Transactions on Electron Devices, ED13(1):164–&, 1966.

[30] C. Lawetz and J.C. Cartledge. *Performance of Optically Preamplified Receivers with Fabry-Perot Optical Filters*. Journal of Lightwave Technology, 14(11):2467–2474, Nov. 1996.

[31] R.C. Steele, G.R. Walker, and N.G. Walker. *Sensitivity of Optically Preamplified Receivers with Optical Filtering*. IEEE Photonics Technology Letters, 3(6):545–547, Jun. 1991.

[32] H. Bülow, F. Buchali, W. Baumert, R. Ballentin, and T. Wehren. *PMD mitigation at 10Gbit/s using linear and nonlinear integrated electronic equaliser circuits*. Electronics Letters, 36(2):163–164, Jan. 20 2000.

[33] K. Azadet, E.F. Haratsch, H. Kim, F. Saibi, J.H. Saunders, M. Shaffer, L. Song, and M.L. Yu. *Equalization and FEC techniques for optical transceivers*. IEEE Journal of Solid-State Circuits, 37(3):317–327, Mar. 2002.

[34] M.D. Feuer, S.Y. Huang, S.L. Woodward, O. Coskun, and M. Boroditsky. *Electronic dispersion compensation for a 10-Gb/s link using a directly modulated laser*. IEEE Photonics Technology Letters, 15(12):1788–1790, Dec. 2003.

[35] O.E. Agazzi, M.R. Hueda, H.S. Carrer, and D.E. Crivelli. *Maximum-likelihood sequence estimation in dispersive optical channels*. Journal of Lightwave Technology, 23(2):749–763, Feb. 2005.

[36] P. Ossieur, C. Mélange, T. De Ridder, J. Bauwelinck, B. Baekelandt, X.Z. Qiu, and J. Vandewege. *Burst-Mode Electronic Equalization for 10-Gb/s Passive Optical Networks*. IEEE Photonics Technology Letters, 20(17-20):1706–1708, Sept.-Oct. 2008.

3

10 Gb/s Burst-mode Transimpedance Amplifier

The PIEMAN BM-Rx consists of an integrated burst-mode PIN-TIA module and a BM-PA chip located at the Optical Line Terminal (OLT) as shown in Figure 3.1. The BM-TIA is the most critical block of a BM-Rx because it should cope with a quick succession of bursts, each with different input power while still providing good sensitivity and large dynamic range. The difference in burst power is a result of different losses in the ODN. The required reaction speed compromises Rx performance.

The designed 10 Gb/s BM-TIA switches its transimpedance gain between two settings to reduce the input dynamic range requirements of the 10 Gb/s BM-PA. The choice of gain is based on the burst input power and the decision is made within 6 ns into the burst. The gain is fixed until the end of the burst. This novel gain locking mechanism avoids burst loss due to a late gain decision.

The specifications of the BM-TIA are given in Section 3.1. Starting from a simple mathematical model, the TIA design is optimized in Section 3.2. An optimum collector bias current and optimum emitter length are chosen to minimize the input-referred noise current. The architecture study is covered in Section 3.3. Both optically differential and electrically differential architectures are considered. The chosen architecture is then explained in detail in Section 3.4. Special attention is paid to the gain switching and locking functions of the TIA. The circuit design of the individual blocks on the TIA is highlighted in Section 3.5. Details of the packaging are given in Section 3.6. This chapter ends with the measurement results in

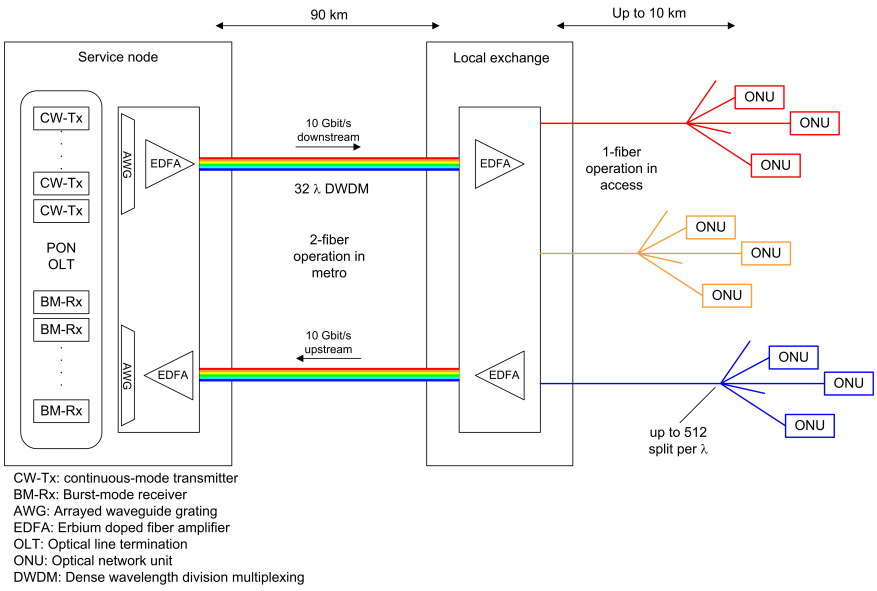

Figure 3.1: PIEMAN network architecture

Section 3.7.

3.1 TIA Specifications

The BM-TIA incoporates the following functionality:

- Conversion from current from the PIN PD into a differential output voltage.
- Low noise amplification and high overload handling.
- Fast automatic gain control on a burst per burst basis.
- Extensive test interfaces for debugging.

A 0.25 μm SiGe BiCMOS7RF technology with carbon doped SiGe heterojunction bipolar transistors (HBTs) was chosen. These HBTs are used for low-noise applications making them ideal for the BM-TIA design. The supply voltage of the BiCMOS7RF technology is fixed at 2.5 V, so originally the supply voltage was specified as 2.5 V $\pm$ 5%. However, the supply voltage limits both sensitivity and DR. Therefore the supply voltage was increased to 2.7 V, which is the maximum allowed supply voltage for the input/output (I/O) cells. A 100 mV resistive voltage drop was taken into account for the resistive drops of the on-chip supply connections yielding a minimum supply voltage specification of 2.6 V. The ambient temperature range was specified from 0 °C to 70 °C.

Parameter	Unit	Min.	Typ.	Max.	Remark
PIN Responsivity	A/W	0.8	0.85	0.9	specified @ 1350 nm
PD bandwidth	GHz	10		13	
PD capacitance	fF		200		
PD serial resistance	Ω	16	20	24	
Bonding inductance	nH		0.7		
Bit rate	Gb/s	5	10		
PIN-TIA sensitivity	dBm,avg	-14	-16	-19	w/o optical preamplification @ BER=10^{-10}, 10 Gb/s
3-dB bandwidth	GHz	8	9	10	
Input referred noise	nArms		1000	1240	ER=10 dB, 0.8 A/W, BER = 10^{-12}
Peak input current	mA	1.8			
Overload	dBm,avg	0			PWD ±15%
Pulse width distortion	%		±10	±15	
AGC run-in time	ns		6	6.4	
supply voltage	V	2.6	2.65	2.7	
Ambient temperature	°C	0	27	70	

Table 3.1: Burst-mode PIN-TIA specifications

The input-referred noise has been derived assuming an ER of 10 dB, a worst-case PIN responsivity of 0.85 A/W (for 1550 nm window), and a BER of 10^{-12}. Note that the required BER for the BM-TIA design itself is 10^{-12} rather than 10^{-10}. Requiring such a low BER was done to ensure sufficient design margin.

As mentioned in Section 2.3.3, chromatic distortion broadens the bit pulses. This causes intersymbol interference (ISI). Besides using dispersion compensating fiber (DCF), electronic dispersion compensation (EDC) [1–4] can be used. The dispersion depends on the ONU transmitting the packet so the electronic equalization parameters will also have to be adjusted from burst to burst. This BM equalization has never been attempted before. The PIEMAN BM-TIA was also intended for research into BM equalization chips outside the scope of the PIEMAN project. This put a strong linearity requirement on the TIA so the TIA could not limit the largest signals. The results of a theoretical study on BM equalization were reported in [5].

The optical amplifiers in the network result in significant amounts of ASE noise. Furthermore, the input signal can be severely distorted due to chromatic

dispersion and polarization-mode dispersion of the metro fibre link. However, for the design, it was assumed that the input signal is not distorted, which can be achieved using DCF or a dispersion compensating module (DCM) and that the OSNR at the Rx is sufficient.

The specifications of the BM TIA are summarized in Table 3.1.

3.2 Transimpedance Amplifier Model

3.2.1 Basic TIA theory

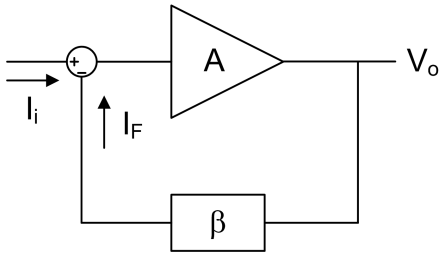

Figure 3.2: Shunt-shunt feedback system

A TIA consists of a forward amplifier with shunt-shunt feedback applied across the amplifier. The input current is converted into an output voltage as a result, which explains the term transimpedance or transresistance. From the Figure 3.2 we can write the output V_o as

$$V_o = A(I_i - I_f). \tag{3.1}$$

With $I_f = V_o\beta$ we can calculate the TIA transfer function to be

$$\frac{V_o}{I_i} = \frac{1}{\frac{1}{A} + \beta}. \tag{3.2}$$

For sufficiently large forward amplifier gain ($A >> 1$) the transfer function simplifies to

$$\frac{V_o}{I_i} = \frac{1}{\beta}. \tag{3.3}$$

In case of a TIA, the feedback path consists of a resistor R_F, so it is easy to see that $\beta^{-1} = R_F$ in (3.3). Thus, the PD current is converted in a voltage with a dc gain R_F. The model for the TIA used above is too simplified. The amplifier A does not have a constant gain with frequency, it will at least have one pole. Its forward transfer function $H_A(s)$ assuming one dominant open loop pole with

corresponding time constant τ_{OL} can be written as

$$H_A(s) = \frac{A_0}{1 + \tau_{OL}s}. \tag{3.4}$$

Substituting Equation (3.4) into Equation (3.2) yields Equation (3.5) for the TIA transfer function.

$$\frac{V_o}{I_i} = \frac{\frac{A_0}{1 + A_0\beta}}{1 + \frac{\tau_{OL}}{1 + A_0\beta}s} \tag{3.5}$$

From (3.5) the closed loop time constant τ_{CL} is found to be

$$\tau_{CL} = \frac{\tau_{OL}}{1 + A_0\beta}. \tag{3.6}$$

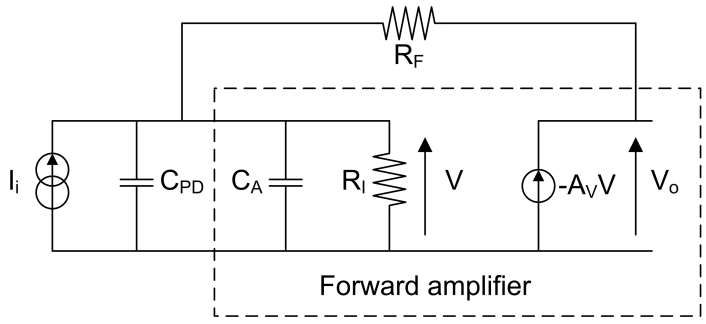

Figure 3.3: General TIA model

Figure 3.3 shows a simple equivalent model of a TIA including PD. The forward amplifier (in the dashed rectangle) is an ideal amplifier with voltage gain A_v. Feedback resistor R_F is also included. In this figure, I_i is the photocurrent, C_{PD} the PD capacitance, C_A the input capacitance of the amplifier, R_I the input resistance of the common emitter (CE) amplifier, V_o is the output voltage of the TIA. With the model in Figure 3.3 one can easily find the TIA's dc-gain A_0 and the open loop time constant τ_{OL}. They are respectively given by Equation (3.7) and (3.8).

$$A_0 = -A_v R_I \tag{3.7}$$

$$\tau_{OL} = R_I C_T \tag{3.8}$$

C_T is the total capacitance at the input node of the forward amplifier, in this case $C_A + C_{PD}$. Using (3.7) and (3.8) and $f_{3dB} = \frac{1}{2\pi\tau_{CL}}$ one finds the bandwidth

f_{3dB} of the TIA equals

$$f_{3dB} = \frac{A_v}{2\pi R_F C_T}, \quad A_v >> 1. \tag{3.9}$$

Equation (3.9) illustrates a basic TIA design trade-off. It shows that the larger the PD capacitance, the smaller the feedback resistor will have to be in case of equal forward amplifier gain. In reality, at 10 GHz, the higher order poles of the amplifier can no longer be neglected. An analysis for a forward amplifier with two poles is given in [6, 7] and will not be repeated here. Also, the influence of the feedback network on the forward amplifier cannot be ignored because the input impedance is finite and the output impedance is not zero. This influence can be included by adding R_F in parallel with R_I for the input loading, and in parallel with the output for the output loading [8].

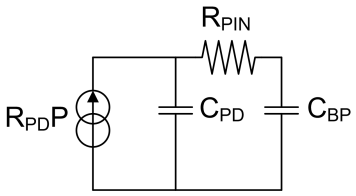

Figure 3.4: Equivalent circuit of the 10 G PIN PD

To add to the problem of analysing and designing a high-speed TIA, the PD high-frequency (HF) equivalent circuit at 10 GHz as shown in Figure 3.4 cannot be simplified to a single capacitance. In this figure R_{PD}, R_{PIN}, C_{PD} and C_{BP} represent respectively the PD responsivity, the PD's dynamic resistance, internal capacitance and bondpad capacitance. On top of all this, the bond wires between PD and TIA and between PD and PD reverse bias circuit will also have an effect on the total transfer function of the TIA. This all makes it very difficult to accurately model a TIA mathematically in order to simplify the design process. An attempt will be made in the following sections, but in the end, designing a high speed TIA requires a number of iterations in the design software, and calculations can only give a starting point from which the software aided design can start, besides giving extra insight.

3.2.2 Noise calculation for TIA with CE front-end

In this section the input referred noise current for a simple HBT CE front-end is calculated. Figure 3.4 shows the equivalent circuit used for the calculations. The total input referred noise current spectrum of a bipolar junction transistor (BJT)

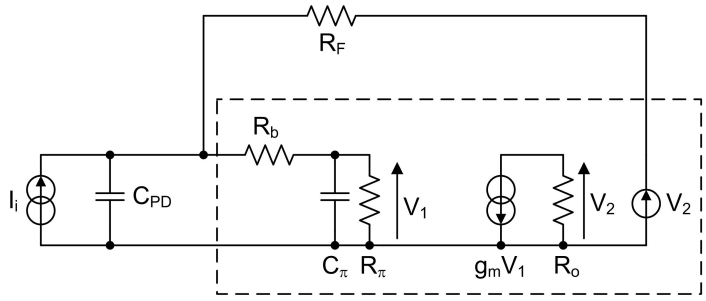

Figure 3.5: Equivalent circuit of CE-TIA

CE front-end is given by equation (3.10) [6].

$$I_n^2 \approx \frac{4kT}{R_F} + \frac{2qI_C}{\beta} + \frac{2qI_C}{g_m^2 R_F^2} + \frac{2qI_C(2\pi C_T)^2}{g_m^2} f^2 + \frac{4kTR_b}{R_F^2} + 4kTR_b(2\pi C_{PD})^2 f^2 \quad (3.10)$$

I_C is the quiescent collector current, β is the current gain of the transistor, g_m is the transconductance of the transistor, R_b is the intrinsic base resistance, C_{PD} is the PD capacitance, C_{BP} is the bondpad capacitance of the PD, R_π is the input resistance of the BJT, C_π is the input capacitance of the BJT and R_o is the resistance at the collector. T is the absolute temperature in Kelvin and k is the Boltzmann constant. The total capacitance at the input of the amplifier is

$$C_T = C_\pi + C_{PD} + C_{BP}. \quad (3.11)$$

The contribution from each noise source in I_n^2 is calculated by transforming its noise spectrum to the output of the preamplifier (multiply by the transfer function from noise source to output voltage) and then calculating it back to the input by dividing the output noise spectrum by the squared amplitude of the preamplifier's transfer function. The intrinsic base resistance of the input transistor has been neglected in the calculation of the noise spectrum terms caused by the collector current shot noise. The first term is the thermal noise of the feedback resistor, the second term originates from the base current shot noise, the third and fourth term are caused by the collector current shot noise and the two last terms are caused by the thermal noise of the intrinsic base resistance. To relate this value to the input referred noise current $\bar{i}_{n,rms}^2$ we should look at the definition of the input referred noise current. It is defined as

$$i_{n,rms} = \frac{v_{n,rms}}{H_0} \quad (3.12)$$

where H_0 is the dc gain value and $v_{n,rms}$ is the root-mean-square value of the output noise of the front-end. From (3.10) it is clear that the spectrum contains a

white component and a component proportional to f^2. So it can be written as

$$I_{n,rms}^2 = \alpha_0 + \alpha_2 f^2. \tag{3.13}$$

Integrating the output noise spectrum and dividing it by H_0^2 yields $\bar{i}_{n,rms}^2$.

$$\begin{aligned} \bar{i}_{n,rms}^2 &= \frac{1}{H_0^2}\int_0^{BW_D} |H(f)|^2 I_{n,rms}^2 \mathrm{d}f & (3.14)\\ &= \frac{\alpha_0}{H_0^2}\int_0^{BW_D} |H(f)|^2 \mathrm{d}f + \frac{\alpha_2}{H_0^2}\int_0^{BW_D} |H(f)|^2 f^2 \mathrm{d}f & (3.15)\\ &= \alpha_0 BW_n + \frac{\alpha_2}{3} BW_{n2}^3 & (3.16) \end{aligned}$$

In these equations BW_D is the detector bandwidth. BW_n and BW_{n2} are called noise bandwidths and are introduced to make the choice of the upper integration boundary BW_D in (3.14) less critical [6]. They are defined as

$$\begin{aligned} BW_n &= \frac{1}{H_0^2}\int_0^{BW_D} |H(f)|^2 \mathrm{d}f & (3.17)\\ BW_{2n} &= \frac{3}{H_0^2}\int_0^{BW_D} |H(f)|^2 f^2 \mathrm{d}f. & (3.18) \end{aligned}$$

A high-speed Rx is constructed as a sequence of blocks with a bandwidth related to the maximum signal frequency. Therefore, the total tansfer function will always have a steep descent. This implies that the integrals in (3.17-3.18) always converge and the resulting noise bandwidths BW_n and BW_{n2} depend only on the preamplifier's transfer function and not on the upper integration boundary BW_D. They can be calculated for some typical transfer functions and are given in Table 3.2 [6].

$\mathbf{H(f)}$	$\mathbf{BW_n}$	$\mathbf{BW_{n2}}$
1st-order low pass	$1.57 \cdot BW_{3dB}$	∞
2nd-order low pass, crit. damped (Q = 0.5)	$1.22 \cdot BW_{3dB}$	$2.07 \cdot BW_{3dB}$
2nd-order low pass, Bessel (Q = 0.577)	$1.15 \cdot BW_{3dB}$	$1.78 \cdot BW_{3dB}$
2nd-order low pass, Butterworth (Q = 0.707)	$1.11 \cdot BW_{3dB}$	$1.49 \cdot BW_{3dB}$
Brick wall low pass	$1.00 \cdot BW_{3dB}$	$1.00 \cdot BW_{3dB}$
Rectangular (impulse response) filter	$0.50 \cdot B$	∞
NRZ to full raised-cosine filter	$0.564 \cdot B$	$0.639 \cdot B$

Table 3.2: Numerical values for BW_n and BW_{n2} [6]

3.2.3 Noise optimization with respect to collector current

The total input referred noise current spectrum as given by Equation (3.10) depends on the collector current I_C. Through the I_C dependence of g_m and C_T, the input referred noise current spectrum becomes a non-linear function of I_C. The relationship between base-emitter junction capacitance C_π and I_C can be written as

$$C_\pi = C_{je} + \frac{\tau_F}{V_T} I_C \tag{3.19}$$

with τ_F the forward transfer time constant of the bipolar transistor, $V_T = \dfrac{kT}{q}$ and C_{je} the zero bias junction capacitance. q is the electron charge. Substituting $g_m = \dfrac{I_c}{V_T}$ and (3.19) into (3.10), α_0 and α_2 can be written as

$$\alpha_0 = \frac{4kT}{R_F} + \frac{2qI_C}{\beta} + \frac{2qI_C V_T^2}{I_C^2 R_F^2} + \frac{4kTR_b}{R_F^2} \tag{3.20}$$

$$\alpha_2 = \frac{2qI_C \left(2\pi \left(\left[C_{je} + \dfrac{\tau_F}{V_T} I_C\right] + C_{PD}\right) V_T\right)^2}{I_C^2} + 4kTR_b \left(2\pi C_{PD}\right)^2 . \tag{3.21}$$

Some terms in Equation (3.20) and (3.21) are proportional to I_C while others are inversely proportional. Therefore an optimum collector current can be found that optimizes the sensitivity, by differentiating the square root of (3.16) and equating the result to zero. The roots of this equation yield the collector currents that generate an extremum in the function $i_{rms}(I_C)$. This gives a general way of finding the optimum collector current of a TIA.

$$\frac{\mathrm{d}\bar{\imath}_{rms}^2}{\mathrm{d}I_C} = \frac{\mathrm{d}\bar{\imath}_{rms}^2}{\mathrm{d}\bar{\imath}_{rms}} \cdot \frac{\mathrm{d}\bar{\imath}_{rms}}{\mathrm{d}I_C} \tag{3.22}$$

$$= 2 \cdot \bar{\imath}_{rms} \cdot \frac{\mathrm{d}\bar{\imath}_{rms}}{\mathrm{d}I_C} \tag{3.23}$$

Because $\bar{\imath}_{rms} \neq 0$ in (3.23) the extrema of $\bar{\imath}_{n,rms}$ are the same as the extrema of $\bar{\imath}_{n,rms}^2$. We will therefore look at $\bar{\imath}_{n,rms}^2$ as a function of the collector current I_C to get insight into the location of those extrema. Both α_0 and α_2 can be written as

$$\alpha_x = \sum_{k=-1}^{1} a_{x,k} I_C^k. \tag{3.24}$$

So we can write

$$\bar{i}_{rms}^2 = \sum_{k=-1}^{1} (a_{0,k} BW_n + a_{2,k} BW_{n2}) I_C^k \tag{3.25}$$

$$i_{rms} = \sqrt{\sum_{k=-1}^{1} (a_{0,k} BW_n + a_{2,k} BW_{n2})\, I_C^k}. \tag{3.26}$$

The values used to calculate the starting value for the noise optimization of the

Parameter	**Value**	**Unit**
T	385	K
R_{PIN}	1	A/W
C_{PD}	290	fF
R_F	650	Ω
BW_n	8.57	GHz
BW_{n2}	10.15	GHz
f_{3dB}	7.5	GHz
β	172	
τ_F	1.98	ps
R_b	7.651	Ω
C_{je}	50	fF
C_μ	4.7	fF
C_{BPC}	35	fF

Table 3.3: Values for calculating the sensitivity vs. collector current

TIA front-end are given in Table 3.3. The first 11 parameters in this table have been previously defined. C_μ and C_{BPC} are respectively the base-collector and TIA bondpad capacitance. Figure 3.6 shows the sensitivity as a function of the collector current, once using (3.19), once with a fixed $C_\pi = 154$ fF. This fixed value is taken from the simulation of the TIA, using standard simulation models. The sensitivity and optimized current in the first case is - 22.7 dBm for 3.31 mA. The latter yields - 23.3 dBm for 6.46 mA. Obviously the collector current influences the sensitivity. Also, both optimization methods yield a different result. The optimization with current dependent C_π gives a starting value for the further optimization of the TIA front-end by means of simulations. This starting value can significantly speed up the total design process. This optimization used the calculated values of BW_n and BW_{n2} as defined by (3.17) and (3.18). Only the bondpad capacitance C_{BPC} of the TIA was taken into account in the simulation and calculation and the bond wire between TIA and PD were ignored.

For the TIA design at 10 Gb/s the equivalent circuit used for the CE amplifier stage in the above equations should be replaced by a HF equivalent schematic like

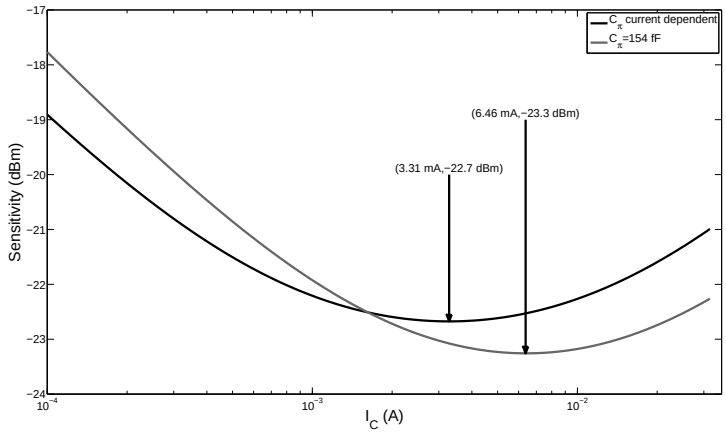

Figure 3.6: Rx sensitivity vs collector current

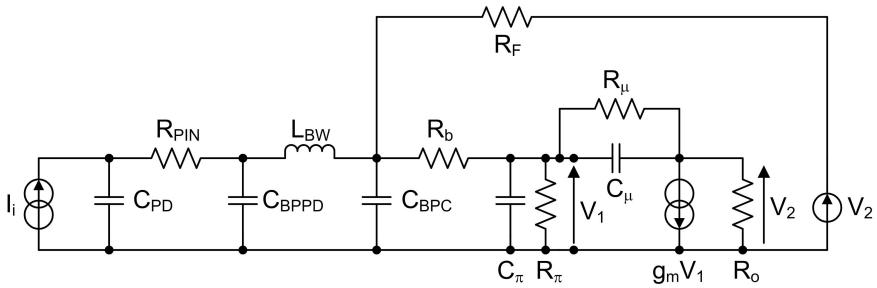

Figure 3.7: PIN-TIA front-end with PD and HF equivalent circuit and PIN-TIA bond wire

the one shown in Figure 3.7. It shows the equivalent circuit of the front-end and PD including the bond wire L_{BW} between PD and TIA. C_{BPPD} is the bondpad capacitance of the PD, C_{BPC} is the bondpad capacitance of the input pad of the TIA die. The bond wire inductance was specified between 500 pH and 900 pH. One can then use this circuit to calculate the input noise current spectrum with the transfer functions of the noise now calculated from the new equivalent circuit. The effect of extra parasitics and PD bond wire can be incorporated by calculating the noise back to the current source of the PD. A high frequency equivalent circuit has more than one pole, and zeros can also be present. In this case (3.16) will not hold anymore because the expression for the input referred noise will no longer be a sum of a constant and f-squared term. The resulting modified Personick integrals [9] have to be calculated from the transfer function in the simulation software.

The current optimization was performed for this high-frequent TIA equivalent circuit including bond wire L_{BW}. The values for this optimization are given in

Parameter	Value	Unit
BW_n	7.34	GHz
BW_{n2}	3.85	GHz
β	251	
τ_F	1.4	ps
C_μ	5.72	fF
L_{BW}	700	pH

Table 3.4: Values for calculating Figure 3.8

Table 3.4. The optimum sensitivity reached by this optimization is -23.1 dBm for a collector current of 2.00 mA. This value is very close the the collector current in the final noise optimized design, as the final current used in the design is 2.03 mA. The calculated transfer function for the optimized collector current including bond

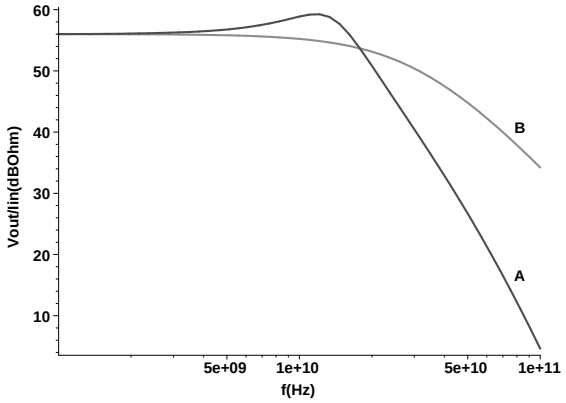

Figure 3.8: Calculated transfer function for optimized collector current (A) including PIN and L_{BW}; and (B) with only C_{PD}

wire and PIN equivalent circuit is given in Figure 3.8 (A - dark grey line), the light gray line (B) shows the transfer function of the TIA calculated without bond wire and with only C_{PD} and the TIA bond pad. As can be seen, the PD and interconnection parasitics give rise to a totally different transfer function, illustrating the importance of including interconnections when designing high-speed TIAs.

3.2.4 Iterative optimization including all parasitics

Figure 3.8 shows that extra bonding parasitics will also cause resonance peaks in the transfer altering the value of BW_n and BW_{n2}. Because the transfer function and BW_n and BW_{n2} are unknown at the start of the design, iterations are required

between current optimization and calculating BW_n and BW_{n2} with the optimized current (and resulting small-signal parameters of the HBT) and then using this value to optimize the noise again. This iteration scheme is shown in Figure 3.9.

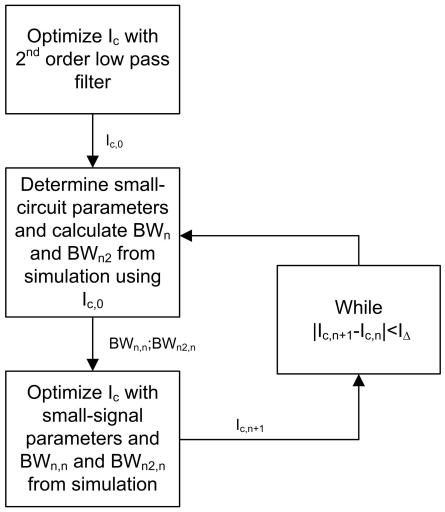

Figure 3.9: Collector current optimization scheme

Conclusions of noise optimization by use of the collector current:

- transfer function and noise spectrum can be calculated for any equivalent circuit of front-end and PD including bonding
- optimization of I_C with Personick integrals yields $I_{c,0}$ (starting value for I_C)
- optimization yields optimum achievable sensitivity
- check of calculated noise and sensitivity in simulation software
- calculated input referred noise can be compared to the noise of other sources (avalanche noise, ASE noise).

3.2.5 Noise matching

As the PD admittance is a parameter in (3.10), it can be chosen in such a way that the input noise of the preamplifier is minimized. For this, a matching network is placed in between the TIA and photodetector to transform the photodetector admittance to the optimum admittance for noise optimization. This is described in [10]. In case of a separate photodetector (as opposed to integrated) the photodetector is bonded to the TIA through a bond wire (L_{BW} in Figure 3.7). This inductance can

be changed to provide the noise matching. Another parameter is the input capacitance of the TIA. The bondpad C_{BPC} will have a certain capacitance value, and one could add on-chip capacitance to help for the matching network.

With only one bond wire, one can provide noise matching at only 1 frequency. The bond wire value required for noise matching at 8 GHz was calculated to be 2.5 nH. The total required input capacitance of the TIA die for noise matching was 550 fF. The resulting integrated output voltage noise was not lower than without the matching network. Higher order matching networks are needed to match the impedance at more frequencies and to reduce the integrated output voltage noise for better sensitivity. However, the module parameters were fixed in PIEMAN, so it was not possible to implement a higher order matching network off-chip. An on-chip matching network would take up too much die area, so noise matching was not implemented in PIEMAN.

3.3 PIEMAN BM-TIA Chip Architecture Study

The PIEMAN BM-TIA linearly amplifies the input currents so offsets are still present at the inputs of the BM-PA. Thus, these offsets can be removed by the BM-PA. The PA expects a differential input signal while the TIA has a single-ended input signal. In this section we study different options to convert the PD current into a differential output signal on the TIA chip. The best architecture for the TIA front-end amplifier is also investigated and it is studied how the large overload specification for the PIEMAN network can be met.

3.3.1 Optically differential TIA front-end

As a consequence of the unipolar nature of light, the optical on-off keying NRZ signal gives rise to a differential offset between both signal phases at the output of the TIA chip. This offset limits the DR and causes a sensitivity penalty and it has to be removed by the BM-PA. Optically differential structures avoid this differential offset by using a dual-PIN detector. Such structures were presented in [11–15]. As shown in Figure 3.10 the Manchester encoded input signal is split into two parts by a Mach-Zehnder Interferometer (MZI). The outputs of this MZI are applied to a dual-PIN PD. The delay between both signals is half a bit period. The splitting ratio is tuned by defining the injection current for the heater of one branch of the MZI. The output of the dual-PIN detector is the difference of the output currents of each PD. The preamplifier converts this current into a voltage which is then high-pass filtered to remove the dc-component. The output of this filter is amplified and limited and the decision circuit (DEC) converts the signals into NRZ-format.

In the PIEMAN network NRZ coding is used instead of Manchester encoding so the architecture of Figure 3.10 was modified to operate with NRZ signals. The

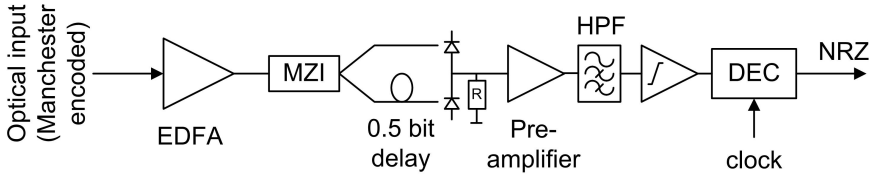

Figure 3.10: Optically differential Rx

resulting architecture is shown in Figure 3.11. The optical NRZ signal is split in half with a MZI and the signal in one of the branches is delayed over half a bit period. The preamplifier amplifies the differential current and turns it into a (differential) output voltage. This is the input for the limiting amplifier. The output is compared to V_{ref} and $-V_{ref}$. The output of the first comparator is the set input of a latch while the output of the second comparator is the reset input of a latch. The output of the latch then gives the reconstructed logical NRZ signal. This is illustrated in Figure 3.12. I_1 is the output of the PD that receives the direct optical signal. I_2 is the output of the PD that receives the delayed optical signal. I_2 is a copy of I_1 but with half a bit period delay. For simplicity it is assumed that the common mode output level of the preamplifier and limiting amplifier are 0 V. In that case V_{ref} = 0 V (assuming there is no noise). The first comparator cuts out all the negative pulses. Similarly, the second amplifier cuts out all the positive pulses. With these two inputs to the latch the original NRZ signal is reconstructed.

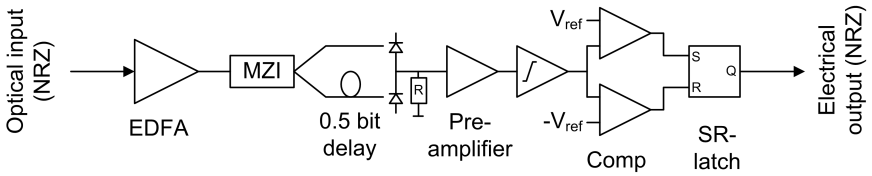

Figure 3.11: Modified optically differential Rx for NRZ optical signals

The above explanation assumes ideal circuits and an ideal incoming signal. Therefore, one should consider some non ideal situations:

- required supply voltages for dual PIN: The input voltage of a TIA is typically temperature dependent and not fixed to 1.25 V. With the on-chip supply voltages being 0 V and 2.5 V, it is difficult to ensure a symmetrical PD bias for both PDs. This is required as the reverse bias determines the responsivity and capacitance of the PD.

- speed: The on-chip operating frequency is doubled because of the half bit period delay. So, the TIA needs a bandwidth of 13 to 15GHz. This is difficult to achieve with the chosen technology.

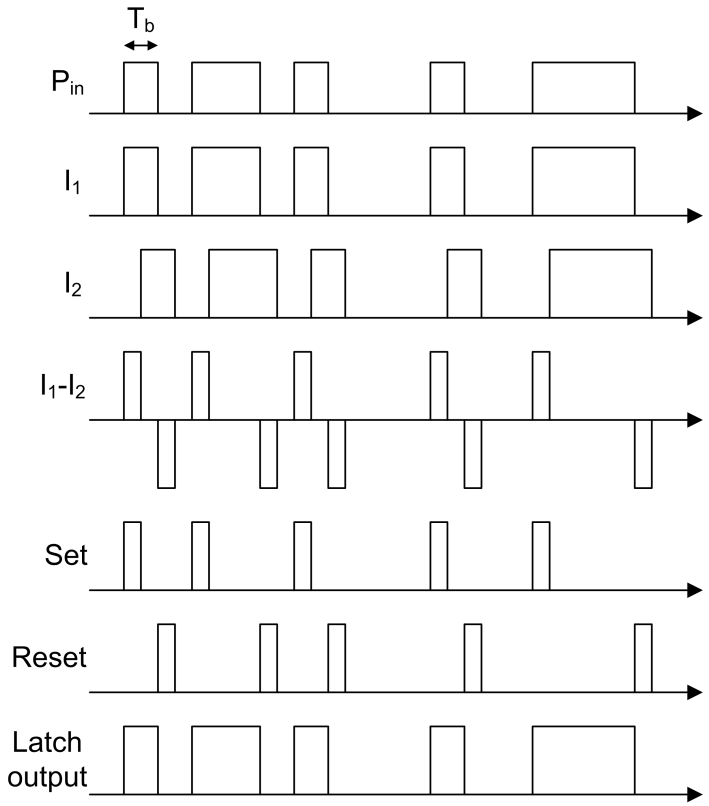

Figure 3.12: Waveforms for an optically differential Rx for NRZ signals

- sensitivity penalties due to responsivity mismatch and non-ideal splitting ratio: The optical coupler splits the optical power into two with a ratio of $(1-r)$:r. This influences the signal at the output of the TIA. Figure 3.13 illustrates this. Part a shows the input current of the TIA in the ideal situation where the $r = 0.5$. Part b shows the situation in case of different splitting ratio, but in case the ER is infinite. Part c shows the input current of the TIA in case of different splitting ratio but with finite ER.
- dispersion: distorted input bits will cause PWD in the output signals.

It is possible to compensate for the difference in responsivity (or for a difference in coupling efficiency to the PDs) by tuning the MZI.

$$I_1 = (1-r)R_{gem}(1+\delta) \quad (3.27)$$

$$I_2 = rR_{gem}(1-\delta) \quad (3.28)$$

R_{gem} is the average responsivity of the photodetectors, δ is the relative difference

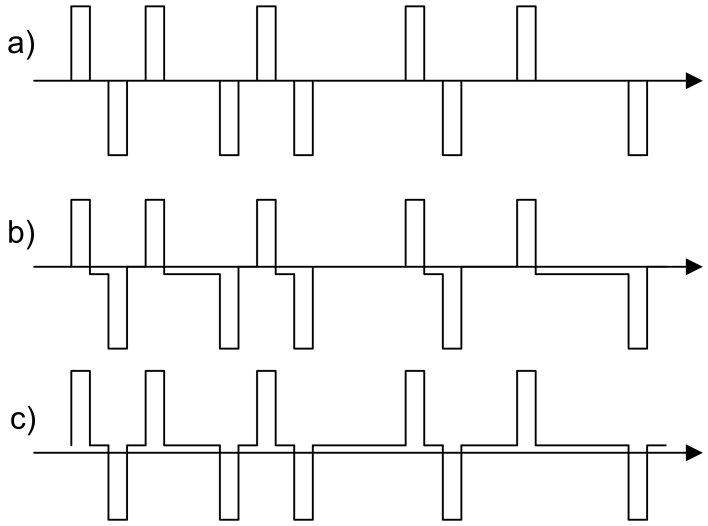

Figure 3.13: Effect of splitting ratio $\neq$ 0.5 on the waveforms for an optically differential Rx

of the responsivity. One can choose r in such a way that I_1 becomes equal to I_2:

$$r = (1 + \delta)/2 \tag{3.29}$$

Tuning the MZI per device is infeasible and impractical and will greatly increase the OLT cost. Both a responsivity mismatch and a non-ideal splitting ratio will lead to a sensitivity penalty.

The required sensitivity for the PIEMAN project is -15 dBm so there is still a margin with respect to the best achievable sensitivity. This architecture has some difficulties decreasing its sensitivity. Firstly, the signal is split into two, with both parts sent to a separate TIA. These two TIAs have in best case the same input referred noise current as a CW-Rx [16]. The state-of-the art CW-Rx at the start of the project had a sensitivity of -19.3 dBm. With the 3 dB penalty due to the signal split this leaves only 1.3 dB for additional BM penalties. With the requirement of the double bandwidth, the integrated output noise will also be larger and an extra penalty will be incurred. From this it is clear that this architecture will not achieve the required sensitivity specification in the chosen 0.25μm technology. The optically differential architecture only works at one operating frequency due to the half-bit delay so the requirement of 5 Gb/s-10 Gb/s dual-speed operation can also not be met.

Another disadvantage is that, as the output state of a RS-latch depends on the previous output for R=S=0, one bit-error might lead to other bit-errors, with a maximum of the maximum CID, see Figure 3.14, dashed line. Other distortions might in turn not cause any bit-error (dotted line) while other distortions cause

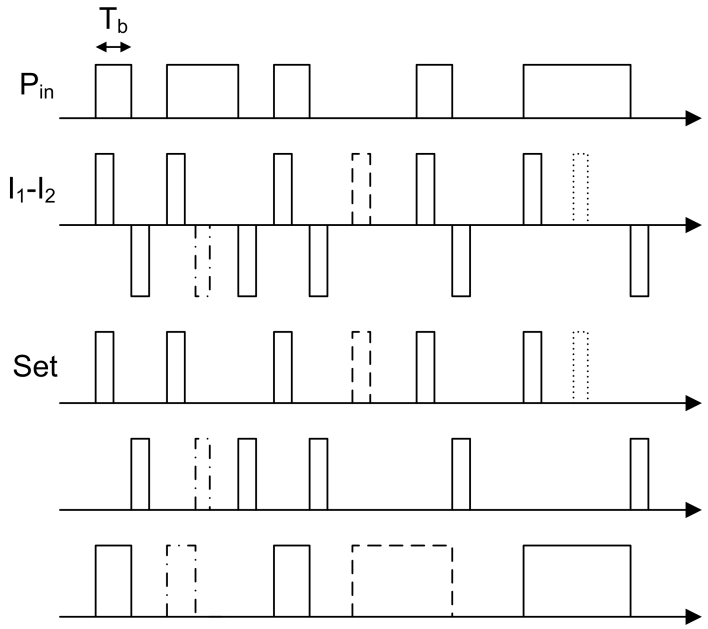

Figure 3.14: Waveforms for optically differential Rx with errors

bit-errors and PWD (dashed-dotted line). Also, an MZI is a highly polarization sensitive device requiring a polarization diversity receiver. Because of the risks involved with this architecture it was not implemented.

3.3.2 Single-ended versus differential TIA

Single-ended signals are very susceptible for disturbances like supply noise, common mode noise and crosstalk. Therefore it is best to convert the single-ended signal to differential signals as soon as possible within the Rx architecture. When an optically differential TIA with dual PIN PD is not an option the conversion to differential signals should be implemented in the electrical domain. Figure 3.15 shows such a fully differential TIA. This architecture is best suited for integrated PDs where a dummy PD that is shielded from the light is easily implemented [17]. When external PDs have to be used, one can either omit the PD and leave the input open or add the PD equivalent circuit on-chip. In both cases the differential TIA will always suffer from the asymmetry in impedance at both input nodes even when the PD is replaced with its HF electrical equivalent. This is because the external bonding cannot exactly be copied on-chip. Besides this impedance asymmetry, a differential TIA contains more components and this inevitably results in more noise. For optimum sensitivity it is therefore best to design a single-ended

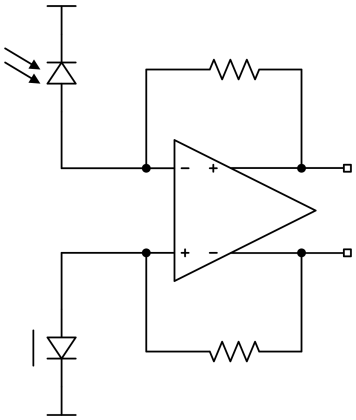

Figure 3.15: Differential TIA

front-end and use a reference as input to the next stage to convert the single-ended signal to a differential signal.

3.3.3 TIA front-end configuration study

A TIA consists of a main (forward) amplifier with a feedback loop closed around it as was shown in Figure 3.2. The feedback path consists of a resistor. Sometimes a capacitance is added in parallel to compensate for unwanted poles. There are three main configurations for this main amplifier. As HBTs in the chosen BiCMOS technology are the only components in the process with sufficiently high transit frequency, only HBT configurations are discussed.

- common-emitter TIA: As this configuration provides both voltage and current gain, this topology gives the best noise performance as long as the bandwidth can be achieved with this configuration.
- common-base: This configuration provides voltage gain but no current gain. The advantage of a common-base TIA is that it shields the PD capacitance from the rest of the circuit [18]. Therefore a higher bandwidth can be achieved with a common-base TIA than with a common-emitter TIA in case the PD capacitance limits the achievable bandwidth. Due to the lower input capacitance of the common-emitter TIA that generally follows the common-base TIA, the feedback resistor can be made larger thus reducing its noise. A drawback is that the common-base input transistor needs bias resistors. The noise of these resistors can only be reduced by choosing large resistors which can be a difficult task in case of a limited supply voltage. As the noise of the feedback resistor is not the dominant noise source in high-speed applications, the reduction of the feedback resistor noise does not compensate for

the extra noise terms added by the common-base transistor and its biasing resistors. Therefore, a common-base TIA is only usefull in high-speed applications where the bandwidth cannot be achieved with a common-emitter TIA due to a large input capacitance.

- common-collector: This configuration only has current gain.

Simulations showed that the bandwidth could be achieved using a CE input stage. Therefore, this stage was chosen.

3.3.4 TIA with large overload

Highest sensitivity requires the maximum value for feedback resistor R_F as indicated by equation (3.10). With this maximized R_F, the TIA will be overloaded for strong bursts. Therefore, the transimpedance gain has to be reduced to meet the DR specifications. Because of the BM operation, this should happen on a burst by burst basis.

There are three ways to combine high sensitivity with a large DR [19]. When an APD is used, the multiplication factor of the APD can be changed to decrease the input current to the TIA [20]. However, this requires complicated fast control circuitry to change the bias voltage of the APD and PIEMAN uses a PIN PD because the signals are already preamplified by the EDFAs. Secondly, one can control the input current [21], but this degrades sensitivity due to the added capacitive load at the input node of the TIA. Thirdly, the gain of the TIA can be decreased by changing the value of the feedback resistor [22–25]. All these methods require detection of the input signal strength which is either done by a comparator with hysteresis or by comparing the peak input level with a predefined voltage reference.

These previous implementations however show two shortcomings. Firstly, a comparator might switch its output very slowly when the signal level has barely crossed the reference level. This is called the minimum overdrive condition of the comparator. A clock can speed up the toggling of the comparator output. Unfortunately, due to the limited pin count of commercial PIN-TIA modules and to avoid cross-talk, a clock is not available on TIAs. Secondly, the input signal of the comparator is noisy. Noise fluctuations can toggle the comparator even if the average of the input signal is below the reference (a non-inverting front-end is assumed in this section). If this occurs after the preamble, the TIA gain can be switched during the transmission of the data payload. This sudden drop in TIA output signal strength will cause malfunction in the BM-PA, because the threshold on the BM-PA is fixed during the data payload after the preamble of the burst. This results in the loss of the burst. An example of this is shown in Figure 3.16 [23]. A BM-PA would interpret all bits after the gain switch as zeros.

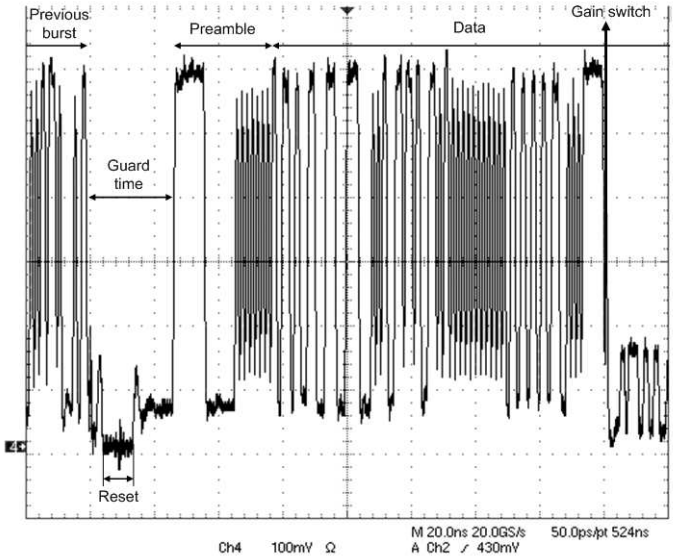

Figure 3.16: Gain switch during data payload

BM-Rx's that use comparators with hysteresis [25] are not free from these issues. If the input signals remain below the threshold level for gain switching during the preamble, noise fluctuations might still toggle the comparator during the burst. It is clear that, for robust operation of gain switching TIAs, the gain must be locked before the end of the preamble to avoid loss of bursts. Therefore, gain locking was implemented on the PIEMAN TIA. This will be explained in Section 3.4.3.

3.4 Chip Architecture of BM-TIA

3.4.1 Top level architecture and building blocks

From the architecture study, a single-ended CE TIA was chosen for high sensitivity. A gain switching functionality was added to combine high sensitivity and large overload. Figure 3.17 shows the implemented top level architecture of the chip. The chip contains 3 main blocks: the datapath, gain switcher and auxiliary circuits. The datapath incorporates a real TIA, a dummy TIA, a Single-ended to differential converter (SE2Diff) and an output buffer. The gain switcher consists of 2 peak detectors (PKDs), 2 comparators, 4 transconductors and some logic. The auxiliary circuits are voltage and current references and test circuits. The dummy TIAs are indicated in gray.

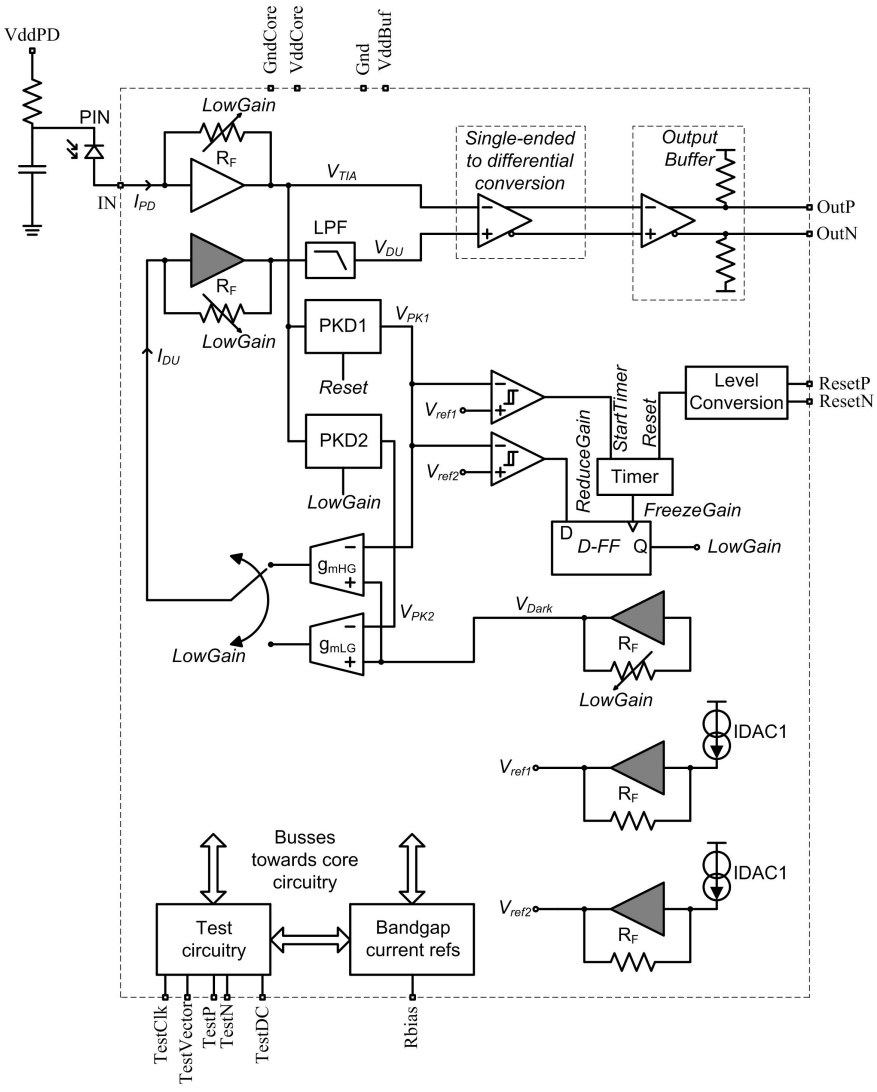

Figure 3.17: TIA toplevel building blocks

A single-ended CE TIA converts the current from the PIN PD into an output voltage. Another (identical) TIA generates a reference voltage that is used in the next stage (SE2Diff) to perform the single-ended to differential conversion. A current-mode logic (CML) output buffer is used to drive the 10 G high-speed I/Os and provide a 50 Ω differential termination for the transmission line connection to the PA.

To cover a wide DR, the gain of the TIA front-end amplifier can be switched

from high gain to low gain at the beginning of the burst. The gain switcher consists of PKD1, 2 comparators, a timer and a data flipflop (D-FF). Its operation will be explained in Section 3.4.2. A threshold is extracted by PKD1, PKD2, 2 transconductors gmHG and gmLG and the dummy TIA. This removes part of the offsets and increases the DR as otherwise the DR would be very limited due to the linearity requirement and limited supply voltage.

3.4.2 Gain switching and coarse threshold extraction

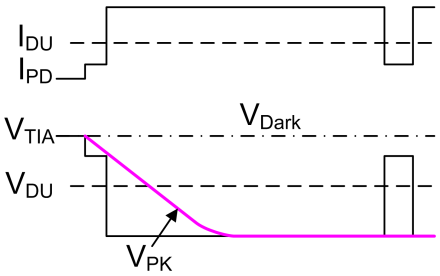

Figure 3.18: TIA signals

The threshold is a coarse threshold because it is based only on the peak level of the '1'. As the guaranteed ER is 10 dB, this means the threshold will not be equal to the optimum threshold [26]. Figure 3.18 shows the input current I_{PD}, preamplifier output voltage V_{TIA}, PKD output V_{PK} and threshold extraction signals V_{Dark}, V_{DU} and I_{DU}. Input current I_{PD} from the PD is converted to voltage V_{TIA} by the TIA front-end with feedback resistance R_F. The peak value V_{PK1} is detected with negative PKD PKD_1. V_{PK1} is used by the gain locking mechanism to determine the value of R_F. The difference between dark level V_{dark} (generated by a dummy TIA) and V_{PK1} is converted into current I_{DU} by a transconductor with transconductance g_{mHG}. This current is then sent into a dummy TIA to create a threshold voltage V_{DU} for the single-ended-to-differential conversion.

If the gain is switched, the gain of the real TIA and two dummy TIAs is switched to low gain and a new peak level V_{PK2} of V_{TIA} is detected by negative PKD PKD_2. $(V_{PK2} - V_{dark})$ is now converted back into current I_{DU} with transconductance g_{mLG}. The transconductances g_{mHG} and g_{mLG} are determined by the requirement that the current I_{DU} is a coarse threshold for the TIA output signal V_{TIA}. So the transconductance value g_m should fulfill

$$g_m R_F \approx \frac{1}{2}. \tag{3.30}$$

As the value of R_F is changed when the gain is switched, g_m should be changed as well.

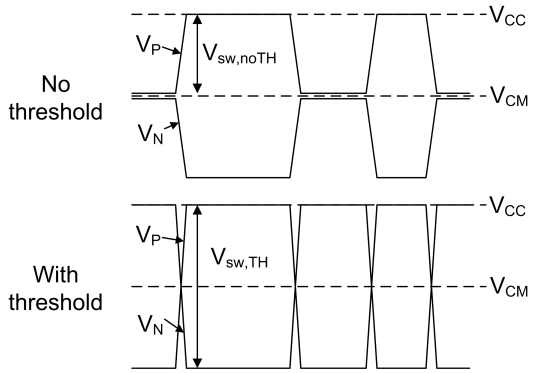

Figure 3.19: Threshold signals

The SE2Diff used a threshold voltage V_{DU} instead of the dark level voltage V_{dark} to increase the achievable DR of the BM-TIA. This is illustrated in Figure 3.19. Because of the limited 2.7 V supply voltage, the maximum input signal swing that can be amplified linearly is limited. Without the coarse threshold extraction, the output signal swing is limited to $V_{sw,noTH}$. As the signals are linearly amplified, we can directly relate this to a maximum input power for a '1' $P_{1,OL}$ (for simplicity we assumed an infinite ER)

$$P_{1,OL} = \frac{V_{sw,noTH}}{A_{SE2Diff}R_{PD}R_F} \tag{3.31}$$

$$= \frac{V_{CC} - V_{CM}}{A_{SE2Diff}R_{PD}R_F} \tag{3.32}$$

where $A_{SE2Diff}$ is the gain of the SE2Diff. With an ideal threshold, we can double $P_{1,OL}$. Thus a coarse threshold extraction was implemented on the BM-TIA. As said in Section 2.1.3. this also removes part of the offset due to the unipolar character of the light. The PKD used in the gain locking block is re-used for the threshold extraction and in this way the extra components needed for this threshold extraction are limited to an extra PKD to detect the new peak when the gain is switched, a dummy TIA and some transconductors.

Also, the threshold is placed in the middle of the signal, and as explained before, in the presence of ASE noise, the optimum threshold is located below the centre of the eye. However, because of the linearity requirement of the TIA, this does not introduce any BM penalty at the TIA level as the data decision is only made in the BM-PA.

The threshold is fed to the SE2Diff using a dummy TIA. As in [27], the threshold could also have been set by directly feeding it to the SE2Diff. The proposed topology however, has superior power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) as both paths to the inputs of the SE2Diff are now

equal. This equality in impedance is slightly disturbed by a low-pass filter (LPF) after the dummy TIA, which is needed to avoid a sensitivity penalty caused the dummy TIA noise.

3.4.3 Gain locking

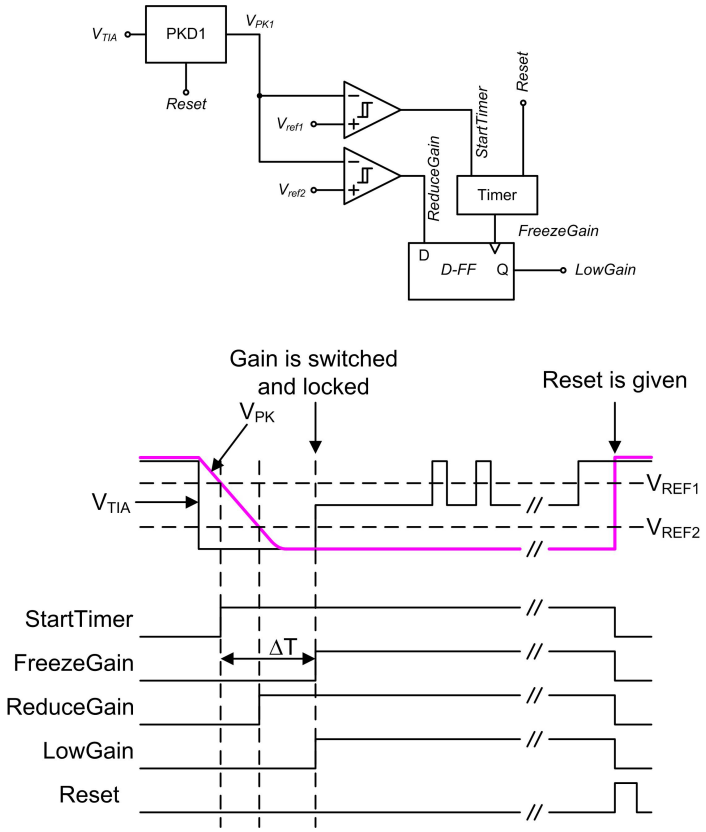

Figure 3.20: Gain switching block and internal signals

The gain setting should be fixed at the start of the burst to avoid a sudden gain change (which may happen if the optical input power drops alongside a burst due to EDFA dynamics). The second purpose of this circuitry is to avoid a 'late' gain decision of the TIA, i.e. a sudden gain switch during the data payload of a burst as was shown in Figure 3.16. This can happen for a signal amplitude close to the transition of high gain to low gain [22] (V_{REF2} in Figure 3.20). Indeed, in this case the peak signal amplitude will be very close to the reference level. This means that the two inputs to the comparator will be very close to each other (minimum

overdrive). In such cases, the comparator delay can be significantly longer than expected (several nanoseconds, even tens of nanoseconds). Noise fluctuations can also trigger a gain change in the middle of a burst because the acquired peak level can drift towards to switching reference during a burst. A timer started at the beginning of the burst to avoid this late switching sets a delay ΔT. After this delay the gain is changed if necessary. Then the gain is frozen. The timer circuit will be explained in Section 4.6.1.

The operation of the circuitry is illustrated in Figure 3.20. The preamble consists of a long string of '1's. During this sequence, the PKD detects the negative peak of the TIA output voltage V_{TIA}. The PKD is a negative PKD because the designed TIA front-end is inverting. This means that the TIA's output voltage decreases with increasing optical input power. The output of the PKD, V_{PK}, is compared to reference levels V_{ref1} and V_{ref2}. V_{ref1} is used to start the timer, V_{ref2} sets the gain switch level. The StartTimer signal becomes high when V_{PK} crosses V_{ref1}. ReduceGain becomes high if V_{PK} also crosses V_{ref2}. LowGain, which regulates the TIA gain, takes on the value of ReduceGain when the timer output FreezeGain becomes high. The D-FF is only reset after the burst so the gain is locked during the data payload.

The total process of reducing and locking the gain should finish within the assigned preamble bits. The most significant delay being incurred is the time that the PKD needs to detect the peak value of V_{TIA}. As will be explained in Section 4.5.1 this depends on the actual peak value and the design of the PKD. Secondly, the comparators have delays. Finally, the glue logic will also incur delays. Even though emitter-coupled logic (ECL)-logic is faster than the standard available CMOS-logic, CMOS logic was chosen for low power consumption. Since the preamble for the BM-PA is significantly longer than the difference in delay between CMOS and ECL-logic, there was no need to increase the gain locking speed by designing the logic in ECL circuits at the expense of higher power consumption and design effort.

The PKD output is erased again during the guard time when the reset signal is high. This successively brings StartTimer and ReduceGain low. The timer itself is also reset, bringing FreezeGain low. The reset of register (D-FF) brings LowGain low at the end of the reset pulse so the BM-TIA is back into HighGain mode, ready for the next burst.

The gain locking system avoids a gain change due to EDFA gain excursions, and late switching of the comparator. For the implementation of the gain locker three other issues needed closer investigation:

- *Minimum overdrive of comparator comparing V_{PK} and V_{ref1}*: As will be explained in Section 3.4.4 this will not cause a faulty gain choice if V_{ref1} and V_{ref2} are spaced sufficiently apart. The gain will be frozen to HighGain somewhere alongside the burst. The gain setting will not change during the

whole burst.

- *Minimum overdrive of comparator comparing V_{PK} and V_{ref2}*: A late decision can of course still happen with the comparator that determines the gain setting itself. This is no problem if a sufficient overlap is ensured between low gain and high gain mode (overlap in the sense of ensuring minimum PWD for the range of input powers).

- *Setup or hold violation of the register*: If the ReduceGain signal changes state at a moment very close in time to the rising edge of FreezeGain, metastability may occur. By carefully choosing the two references, the speed of the PKD and the length of the timer, it is possible to limit the chance of occurrence for this situation.

All references used in the gain-switching mechanism are generated using replica TIAs to increase the robustness of the gain switching and locking mechanism against process, supply and temperature variations.

3.4.4 Gain locker analysis

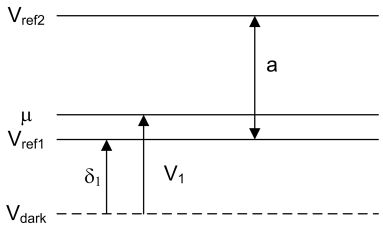

Figure 3.21: Gain switching and locking references

For the analysis we will consider a TIA with *non-inverting* front-end (so the TIA output increases with increasing optical power). The noise on the one-level is assumed to be a Gaussian process with mean μ and variance σ^2. The relevant voltage levels are shown in Figure 3.21. V_{dark} is the output level of the TIA without optical input power, V_{ref1} and V_{ref2} are the gain switching references, and μ is the average of the TIA output voltage during the preamble. The average number of upcrossings per time unit $\mu^+(u)$ (called the upcrossing intensity) is proportional to [28]:

$$\mu^+(u) \sim e^{-\frac{(u-\mu)^2}{2\sigma^2}}. \tag{3.33}$$

With

$$\mu = V_{dark} + V_1 \tag{3.34}$$
$$V_{ref1} = V_{dark} + \delta_1 \tag{3.35}$$
$$V_{ref2} = V_{ref1} + a \tag{3.36}$$

the ratio ρ of upcrossings to level V_{ref2} to upcrossings to level V_{ref1} is given by

$$\rho = \frac{\mu^+(V_{ref2})}{\mu^+(V_{ref1})} = exp\left(-\frac{a\,(2\,(\delta_1 - V_1) + a)}{2\sigma^2}\right) \tag{3.37}$$

Table 3.5 shows ρ for different $\delta_1 - V_1$ and a for $\sigma = 4$ mV (rms noise at the output

$\delta_1 - V_1$	**0.5 mV**	**1 mV**	**2.5 mV**	**5 mV**	**10 mV**
$a = 10mV$	3.2e-2	2.3e-2	9.2e-3	1.9e-3	8.4e-5
$a = 20mV$	1.9e-6	1.1e-6	1.6e-7	7.2e-9	1.39e-11
$a = 30mV$	2.4e-13	9.4e-14	0	0	0

Table 3.5: Ratio of upcrossings to two different voltage levels

of the TIA calculated from -16 dBm sensitivity, 0.85 A/W and Q=6.31). From this table it is clear that there are significantly more upcrossings up to V_{ref1}. When a is sufficiently large, it is very unlikely that both comparators will switch late. In the final design $a = 100$ mV so it is therefore almost impossible to have a switch of gain during the data payload of the burst.

Compared to [23] this method effectively reduces the chance of a gain switch during the data payload. As in [23] the detected peak can acquire noise peaks during the complete burst, there is a real chance of crossing the gain switching reference. While now, the acquired noise peaks should cross both references within a much shorter time frame to trigger a late gain switch. As shown before, this is extremely unlikely if the references are carefully chosen.

3.5 Circuit Design of 10 Gb/s BM-TIA

3.5.1 TIA front-end

Figure 3.22 shows the circuit of the BM-TIA front-end. It consists of a CE stage (Q_1) which provides the open loop gain and a follower (Q_6) to provide a low impedance to the feedback loop. The feedback circuit consists of 3 resistors, R_2, R_3 and R_4, all equal to 650 Ω. C_1 creates a zero that cancels out an unwanted pole of the forward amplifier. Switch M_3 does not conduct in high gain mode. The current from M_2 flows to ground because Q_2 is conducting and Q_3 is not conducting in high gain mode. The transimpedance gain is approximately equal

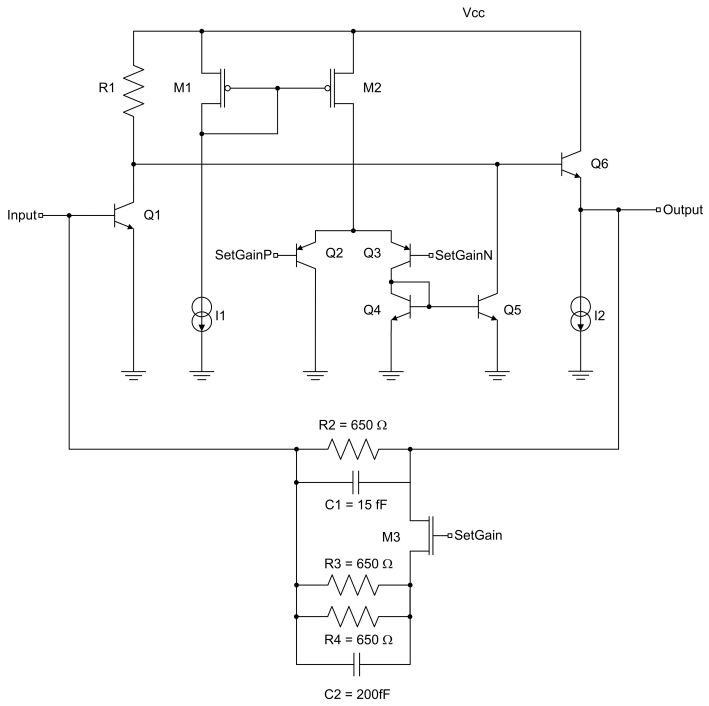

Figure 3.22: TIA front-end circuit

to R_2. Switch M_3 conducts in low gain mode reducing the transimpedance gain by approximately a factor 3. Capacitor C_2 is added to reduce the open loop gain for high frequencies to ensure stability. Also, the differential pair is now driven to send the current from M_2 to Q_4 where it is mirrored to Q_5. This lowers the transconductance of Q_1, which in turn decreases the forward gain improving stability.

The high gain transimpedance value R_{FH} is equal to 650 Ω, the low gain transimpedance value $R_{FL} = 216\,\Omega$. The output voltage of the TIA is equal to

$$V_{TIA} = V_{be} - R_{FL} I_{in}. \tag{3.38}$$

V_{TIA} should remain above the saturation voltage of the current source transistor (I_2) to avoid excessive PWD. Therefore, an upper limit on R_{FL} is imposed by the maximum input current specification. For a 350 mV saturation voltage this means $R_{FL} < 250\,\Omega$ with $I_{in,max} = 1.8$ mA (3.1). The choice of R_{FH} was described previously. The corner variations and PD parameter variations limited the value for R_{LH} further than calculations indicated. A parallel feedback network was chosen because of the need for C_2. As shown in Figure 3.23 a series feedback network requires two switches. Although the latter approach leads to a lower capacitance on

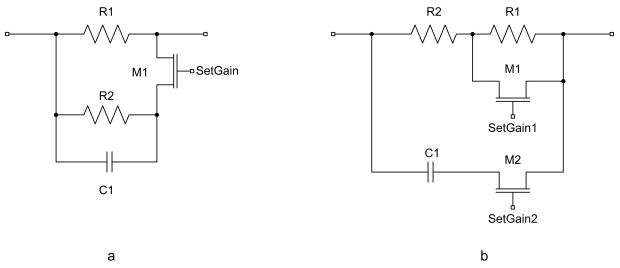

Figure 3.23: Feedback network: parallel (a) and series (b)

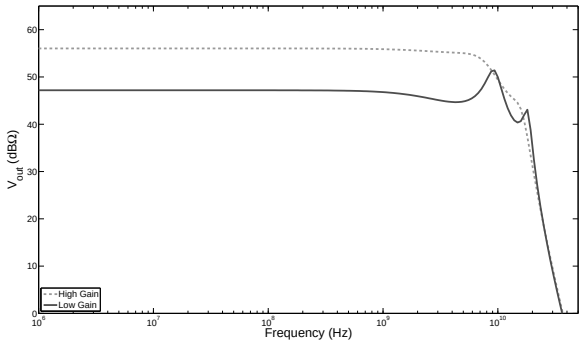

Figure 3.24: Simulated transfer function of TIA for high gain (dotted line) and low gain (solid line) setting

the input node of the TIA, the two switch requirement involves a risk of instability. It is almost impossible to toggle two switches at exactly the same time. The TIA becomes unstable if the resistor is already short-circuited and the capacitor is not yet connected. This results in a fairly long transient requiring a longer preamble.

The simulated transfer function of the TIA core in high gain (dotted line) and low gain (solid line) is plotted in Figure 3.24. The simulation includes the extracted parasitics of the layout and the PD equivalent circuit and its connection to the TIA die. The dc gain in high gain and low gain setting is respectively 56 dBΩ and 47.2 dBΩ. The low gain transfer function has two resonance peaks at high frequencies caused by the bonding and PD parasitics. The effect of these resonances is mitigated by the transfer function of the subsequent blocks in the datapath.

Figure 3.25 shows the simulated high gain transfer function of the front-end with (solid line) and without (dashed line) input bond wire. Clearly, the TIA was designed in such a way that its transfer function compensates for the resonance peak caused by bond wire and C_{BPPD} and C_{BPC}. The transfer function of TIA alone does not have sufficient bandwidth. The bandwidth specification is met by

use of the bond wire resonance peak.

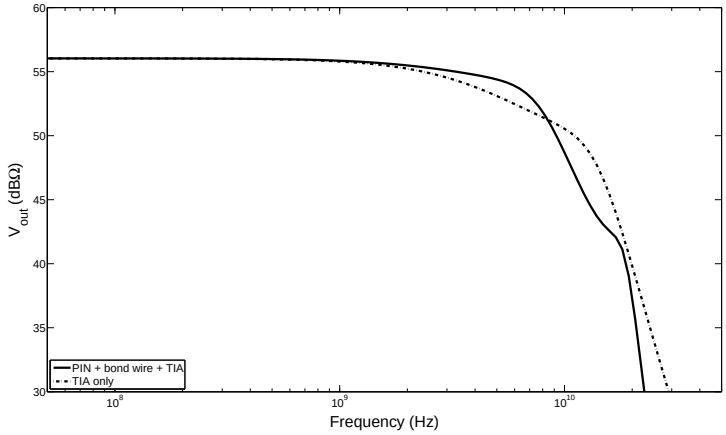

Figure 3.25: Tranfer function of TIA for PIN + bond wire; TIA only

3.5.2 Transconductors

The transconductor is shown in Figure 3.26. The transconductance G_M can be approximated by

$$G_M = \frac{1}{R_5}. \tag{3.39}$$

This follows from the fact that due to the differential nature of the circuit, one half of the circuit can be regarded as a CE with current feedback. Equation (3.39) is only valid for large loop gain A_{OL}, which equals

$$A_{OL} = g_m \left(\frac{1}{\frac{1}{2R_5} + \frac{1}{r_\pi}} \right). \tag{3.40}$$

If r_π is sufficiently larger than R_5 A_{OL} is simplified to $2g_m R_5$. (g_m and r_π are the small signal parameters of $Q1$ and $Q2$. The threshold circuits require that Equation (3.30) is fulfilled by G_M. It was difficult to design the circuit such that the A_{OL} was sufficiently large. Therefore the transconductance of the circuit differs slightly from the value given by Equation (3.39). Since A_{OL} becomes even smaller for the low gain setting, it was decided to use three identical transconductors to generate the threshold current in the low gain setting. So in total the block in Figure 3.26 is used 4 times. A differential pair is used to switch between the high gain dummy current (output of 1 transconductor) or low gain dummy current (output of 3 transconductors in parallel).

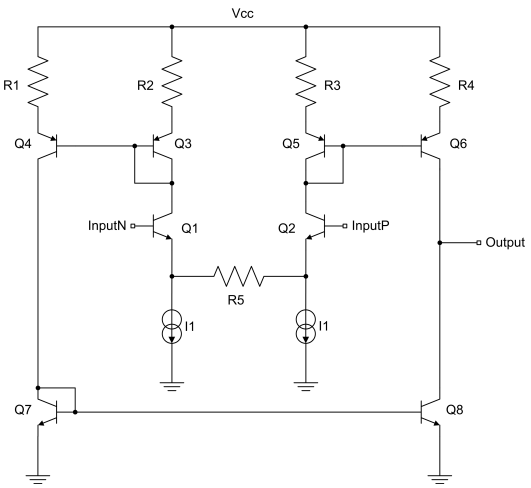

Figure 3.26: Transconductor circuit

3.6 Packaging of 10 Gb/s PIN-TIA Module

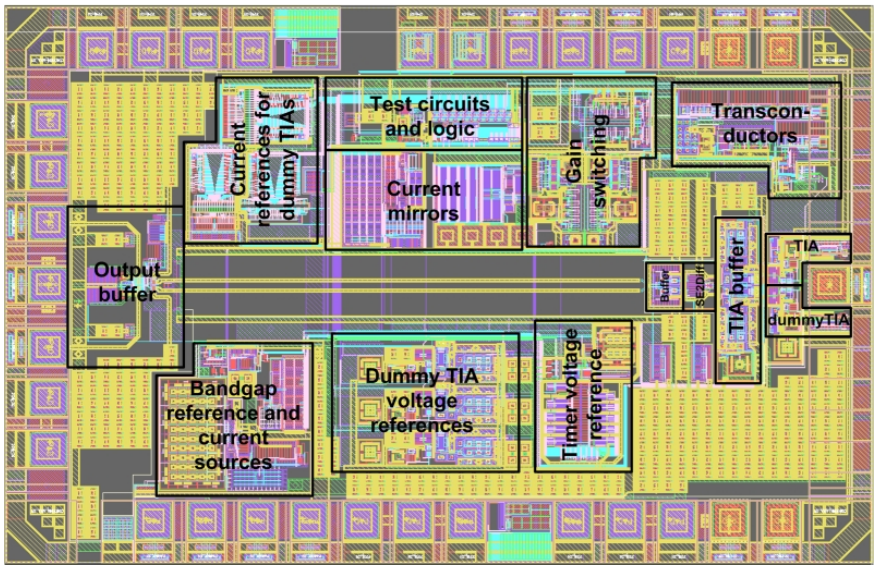

Figure 3.27: 10 Gb/s TIA layout

Figure 3.27 and 3.28 show the layout respectively and the die micrograph of the TIA. The die measures 1.8 mm by 1.2 mm. The right bondpad is the input bondpad that is connected to the PIN PD. To keep this bond wire as short as possi-

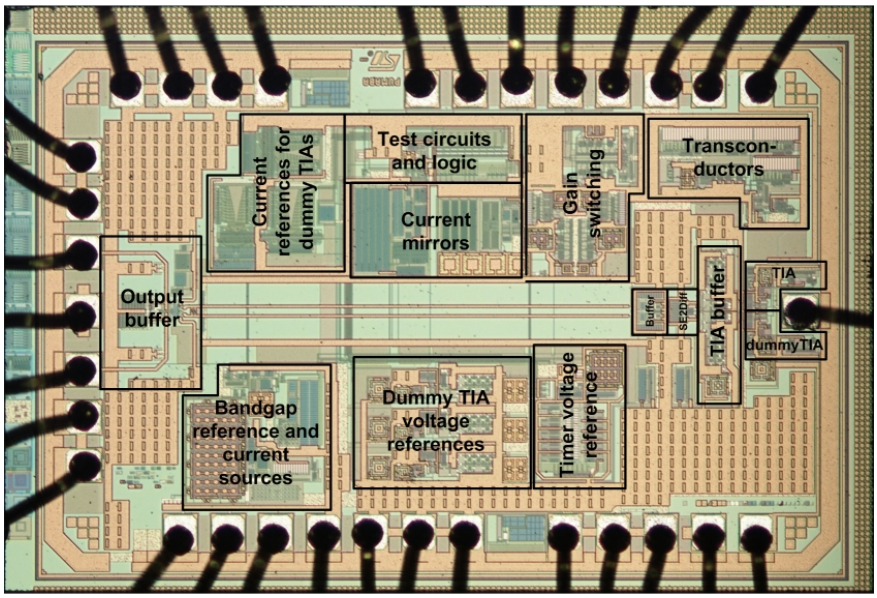

Figure 3.28: 10 Gb/s BM-TIA die micrograph

ble, no other bondpads were placed on the input side (right side on micrograph) of the die. This also avoids coupling between the input signal and other signals that are connected to traces on the substrate in the module. The differential outputs are located at the opposite side of the die. This reduces crosstalk from output to input. The TIA and dummy TIA are located closest to the input bond pad. These two blocks are followed by a TIA buffer made up from PNP followers that shift the signals upwards so they fit within the input common mode range of the SE2Diff. Next comes the SE2Diff and an extra buffer. The output buffer is located at the other end of the die to minimize the length of the output traces. The connection between buffer and output buffer input is made with metal tracks, whose dimensions are chosen such to minimize the effects of the parasitics of these lines. The area nearest to these tracks is kept empty of metal to reduce the tracks' capacitance to other signals. The transconductors are located close to the TIA cores to limit the capacitance of the trace to the dummy TIA. The gain switching was also put as close as possible to the TIA cores. The other blocks are voltage and current references, test circuits and logic. About 12% of the die area is filled with supply decoupling capacitors, to decouple high speed disturbances directly on-chip.

Figure 3.29 shows the 10 G PIN-TIA module. The components within this module are:

- A 10 Gb/s PIN diode: Planar InGaAs/InP with 34 μm diameter PIN PD (CDP-P34) from HG Genuine

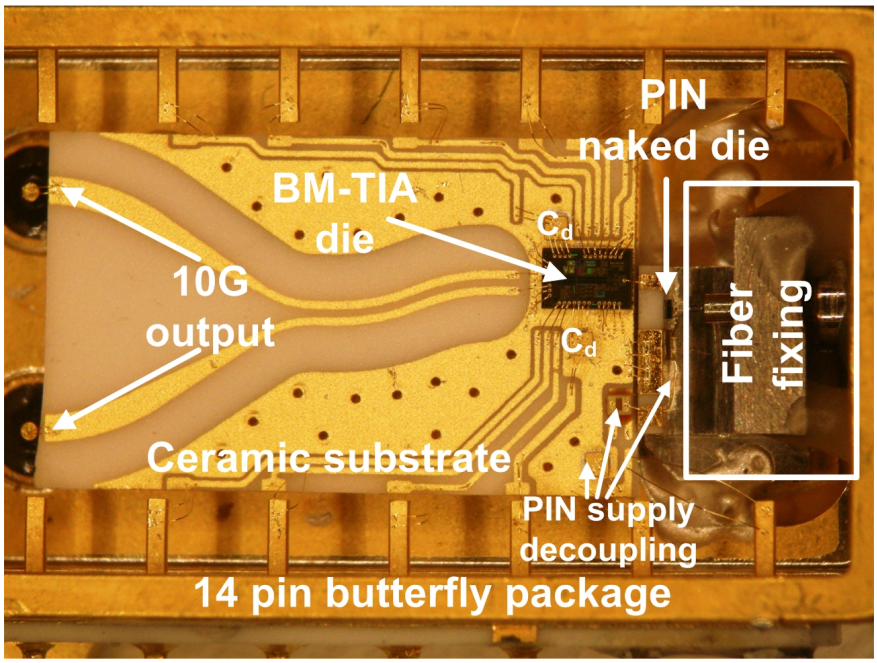

Figure 3.29: 10 G PIN-TIA module

- An alignment structure to couple the optical power from the fiber onto the PIN diode
- A substrate to mount the TIA die and decoupling capacitors
- 10G transmission lines for interconnections between the BM-TIA and the BM-PA integrated circuit (IC).

The BM-TIA was integrated together with the 10 G PIN PD and assembled into a butterfly package with an alignment structure that fixes the fiber position. The TIA was mounted on a substrate together with some decoupling capacitors (C_D) (see Figure 3.29). The PD is mounted on a ceramic block with gold interconnections and tilted towards the fibre. On this ceramic block, an additional decoupling capacitor is placed. The fiber alignment block is put as close as possible to the TIA die to keep the input bond wire as short as possible. The fiber alignment block was designed to have the same height as the substrate and TIA die together, minimizing the bond wire length. Attention was paid to the following points during the design of the I/O-ring:

- Use of a large number of ground and supply pads, to keep the impedance of these connections as low as possible.

- Placing input and outputs as far apart as possible, and symmetrical with respect to each other.
- Placing the different supply domains as far apart as possible.
- Placing respective ground and supply connections close to each other on the module facilitating decoupling.
- Placing components and traces in such a way to ensure the smallest possible bond wires for supply, ground, input and outputs.

3.7 Test Setups and Measurements

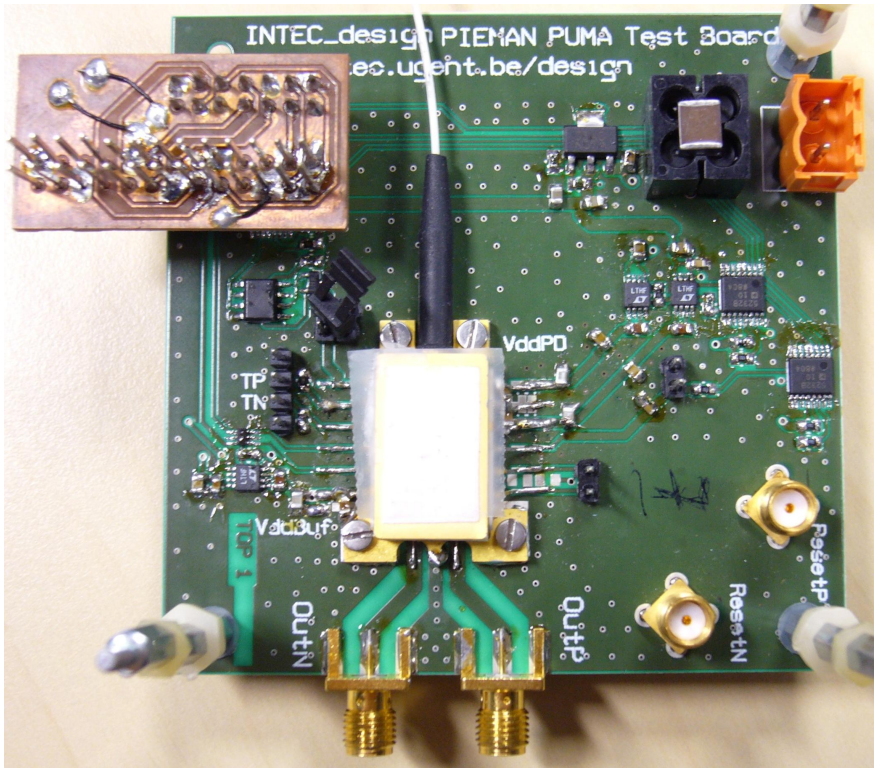

Figure 3.30: 10 G PIN-TIA PCB

Figure 3.30 is a photograph of the PCB designed to test the 10 G PIN-TIA module. The 10 G PIN-TIA module is soldered onto a conductive surface on the ground plane of the PCB to ensure a good ground connection. The 10 G outputs are connected to two SMA connectors through 50 Ω transmission lines. The reset

signals are connected to the PCB through SMA connectors ResetP and ResetN. Headers were used for easy testing access. The small PCB on top of the PIN-TIA module PCB is a patch board designed in INTEC_design to integrate BM-TIA, BM-PA and BM-CDR into one setup where all three test boards' settings were programmed using one microcontroller.

At 10 Gb/s, the electrical interface between the PIN PD and the BM-TIA chip is extremely critical. During the design phase, it became clear that in order to ensure performance and stability of the TIA, detailed electromagnetic modeling of the bond wires is necessary. The interconnection has been modeled using FastHenry software, which was especially developed for this purpose [29]. This software allows to input the geometrical structure of the TIA interconnections and bond wires, and generate an equivalent SPICE model of these interconnections. Inductance, coupling inductances, resistance and skin effect of the interconnections are all taken into account.

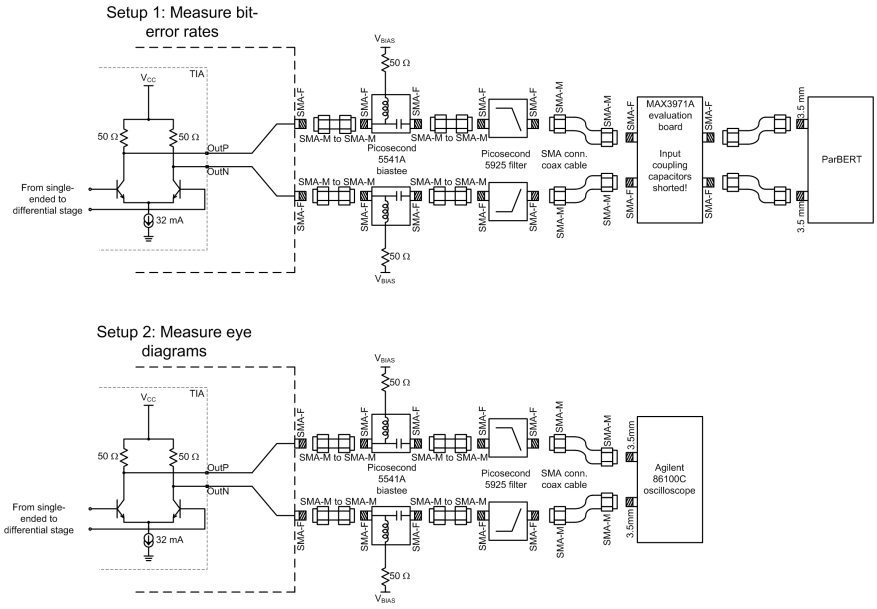

Figure 3.31: Test setups for 10 G PIN-TIA module

Two test setups were configured to test the performance of the TIA. These are shown in Figure 3.31. The supply voltage V_{bias} is the same voltage as the supply voltage of the output buffer. The TIA is connected through a bias-tee to a 50 Ω termination to the output buffer supply voltage. The ac-coupled signal can then be filtered if necessary and either be viewed on the scope, or connected to a CW-limiting amplifier [30] to measure bit-error-rates.

During testing two problems were found. The first problem is that one of the

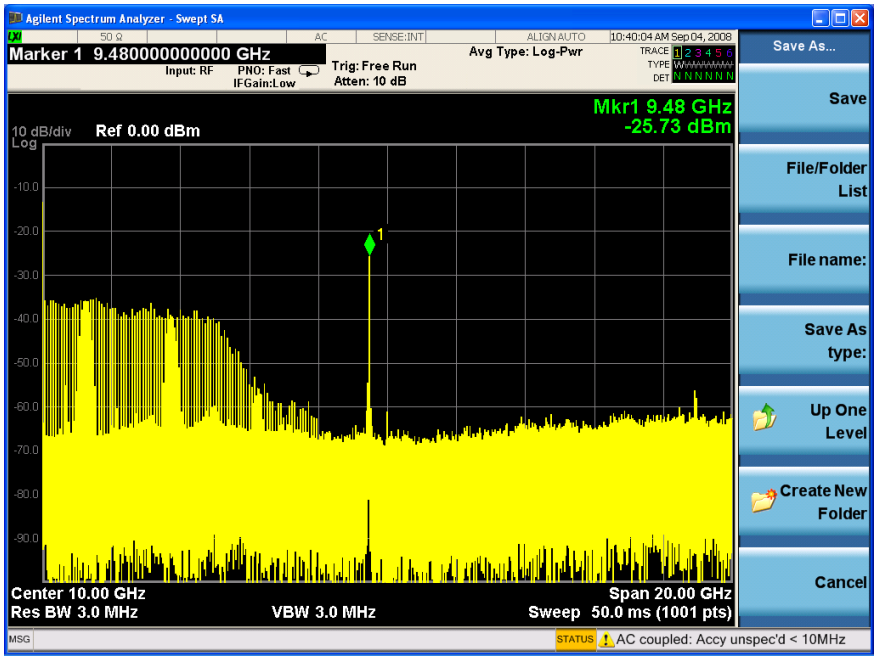

Figure 3.32: TIA output spectrum without optical input power - pre-FIB

two modules showed an oscillation at around 9.5 GHz when high gain is set for the TIA. The output spectrum measured without optical input power is shown in Figure 3.32. This problem was caused by feedback paths and resonances occurring through the bond wires of the power supplies. The solution suggested by colleagues was to connect two originally separated ground domains (input and output stages) together directly on the TIA die via a Focused Ion Beam (FIB) operation. The oscillation was eliminated completely on this module after this FIB operation.

The second problem is additional Inter-Symbol Interference (ISI) and Data Dependent Jitter (DDJ). Intensive simulations have been carried out within the Intec_design team using non-linear accurate transistor models, and including all layout details and all bond wires. Such post-layout simulations are very time-consuming and could not be performed before chip manufacturing due to time restrictions. Additional investigations were performed also including the contributions of substrate transmission lines, bonding to the module pins, transmission lines on the test PCB and SMA connectors. The extra ISI and DDJ are mainly caused by unsatisfactory PIN PD decoupling, due to the fact that the PIN and the TIA die have a separate substrate and a carrier respectively in the PIN-TIA module as can be seen in Figure 3.29. The voltage on the photodiode cathode is not decoupled well enough due to parasitic inductance of the bonding. This extra ISI

and DDJ made it impossible to test the BM-TIA with pseudo-random bit sequence (PRBS)-sequences with an order above 15.

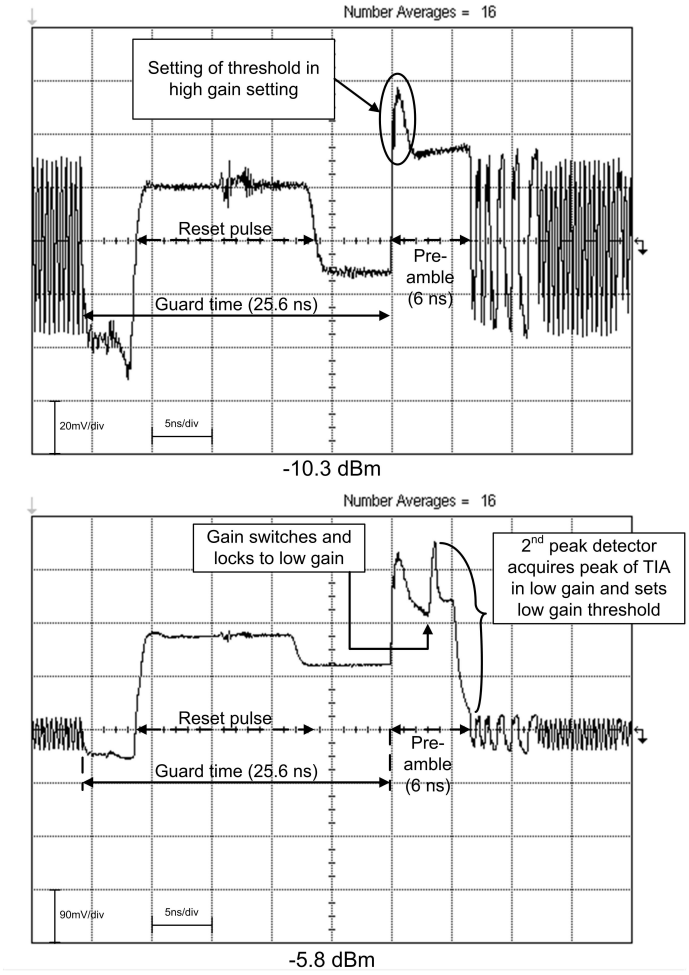

Figure 3.33: Transient results

Figure 3.33 illustrates the transient outputs at the beginning of a burst. On the left side of the figures, the end of the previous burst is shown, then the guard time is observed during which a reset signal is received. The effect of the reset pulse is clearly visible in the outputs of the TIA. At the end of the reset pulse, the PKDs start acquiring the level present just before the start of the burst. The upper figure shows the differential output of the TIA when receiving a burst with average optical input power of -10.3 dBm. The peak at the start of the preamble

is the threshold being acquired. The lower figure shows the differential output of the TIA when receiving a burst with average optical input of -5.8 dBm. Again we see a peak at the beginning of the preamble that is due to the threshold being acquired. At approximately 3.5 ns the gain is switched and locked and a second peak is visible. That peak is due to the second PKD acquiring the peak level of the preamplifier output, and the threshold being set. The time needed for the TIA to settle to low gain and the threshold extraction circuits to settle is about 6 ns.

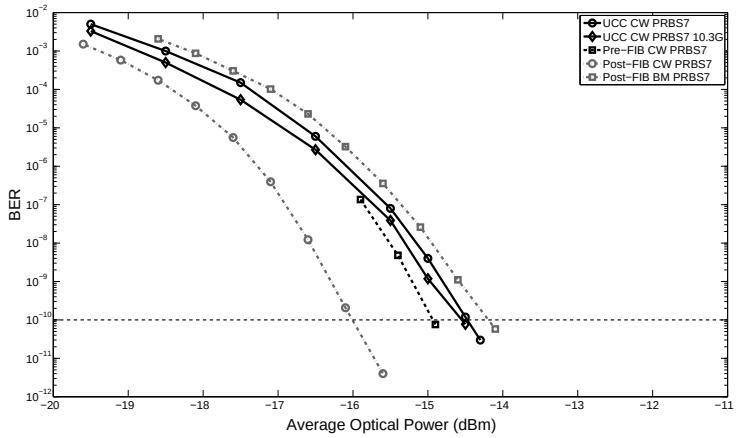

Figure 3.34: Measured BER curves TIA (PRBS7)

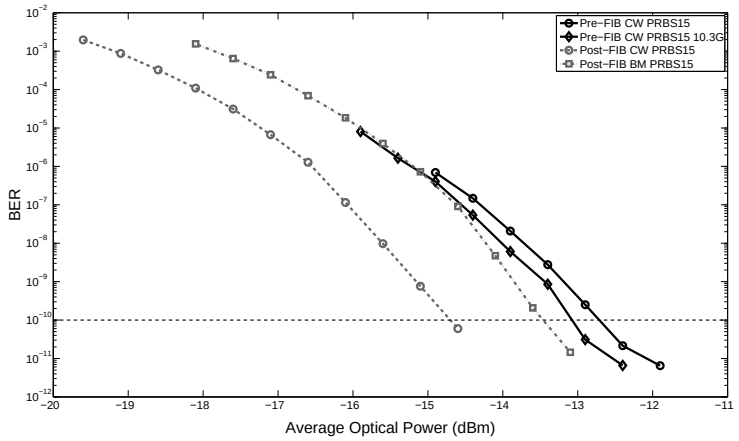

Figure 3.35: Measured BER curves TIA (PRBS15)

BER measurements were performed on two different TIA test boards and in

two different locations. The resulting BER curves are shown in Figure 3.34 and 3.35 respectively.

The results in Figure 3.34 have been produced using a PRBS $2^7 - 1$ sequence. The continuous mode measurements were performed by fixing the gain to high gain and the dummy TIA input current was manually set to zero. In this test mode, the gain switcher block is obsolete. The gain switcher was used for the BM measurements. The BM penalty at a BER of 10^{-10} is 1.8 dB. The measurements of Board 6 at University College Cork (UCC) and Board 5 at INTEC before the focussed ion beam (FIB) operation show similar performance. After FIB, the sensitivity is increased by 1.1 dB.

Figure 3.35 gives the results by using a PRBS $2^{15} - 1$ sequence. The BM penalty is now 1.2 dB. Again, FIB improves the performance, now by 2 dB.

The sensitivity results are given in Table 3.6. Before the FIB operation it was impossible to test board 5 in BM operation. Board 6 was only tested in CW with a PRBS7 sequence without the BM-PA.

The overload of the TIA alone was not evaluated. The results of the total BM-Rx (BM-TIA+BM-PA) will be given in Chapter 4.

	INTEC Board 5 (before FIB)	**INTEC Board 5 (after FIB)**	**Board 6 (at UCC)**
PRBS7 - CW	-14.9 dBm	-16.0 dBm	-14.5 dBm
PRBS7 - BM	N.A.	-14.2 dBm	N.A.
PRBS15 - CW	-12.7 dBm	-14.7 dBm	N.A.
PRBS15 - BM	N.A.	-13.5 dBm	N.A.

Table 3.6: Measured PIN-TIA sensitivities (two modules) at 10 Gb/s

References

[1] H. Bülow, F. Buchali, W. Baumert, R. Ballentin, and T. Wehren. *PMD mitigation at 10Gbit/s using linear and nonlinear integrated electronic equaliser circuits*. Electronics Letters, 36(2):163–164, Jan. 20 2000.

[2] K. Azadet, E.F. Haratsch, H. Kim, F. Saibi, J.H. Saunders, M. Shaffer, L. Song, and M.L. Yu. *Equalization and FEC techniques for optical transceivers*. IEEE Journal of Solid-State Circuits, 37(3):317–327, Mar. 2002.

[3] M.D. Feuer, S.Y. Huang, S.L. Woodward, O. Coskun, and M. Boroditsky. *Electronic dispersion compensation for a 10-Gb/s link using a directly modulated laser*. IEEE Photonics Technology Letters, 15(12):1788–1790, Dec. 2003.

[4] O.E. Agazzi, M.R. Hueda, H.S. Carrer, and D.E. Crivelli. *Maximum-likelihood sequence estimation in dispersive optical channels*. Journal of Lightwave Technology, 23(2):749–763, Feb. 2005.

[5] P. Ossieur, C. Mélange, T. De Ridder, J. Bauwelinck, B. Baekelandt, X.Z. Qiu, and J. Vandewege. *Burst-Mode Electronic Equalization for 10-Gb/s Passive Optical Networks*. IEEE Photonics Technology Letters, 20(17-20):1706–1708, Sept.-Oct. 2008.

[6] E. Säckinger. *Broadband Circuits for Optical Communication*. John Wiley & Sons, 2005.

[7] J. Verbeke. *Studie en Ontwikkeling van een Breedband Elektro-Optische Interconnectietechnologie*. PhD thesis, 1995.

[8] P. Gray, P. Hurst, S. Lewis, and R. Meyer. *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 2001.

[9] J.J. Morikuni, A. Dharchoudhury, Y. Leblebici, and S.M. Kang. *Improvements to the Standard Theory for Photoreceiver Noise*. Journal of Lightwave Technology, 12(7):1174–1184, Jul. 1994.

[10] M.S. Park and R.A. Minasian. *Ultra-Low-Noise and Wide-Band-Tuned Optical Receiver Synthesis and Design*. Journal of Lightwave Technology, 12(2):254–259, Feb. 1994.

[11] H. Nishizawa, Y. Yamada, K. Habara, and T. Ohyama. *Design of a 10-Gb/s burst-mode optical packet receiver module and its demonstration in a WDM optical switching network*. Journal of Lightwave Technology, 20(7):1078–1083, Jul. 2002.

[12] Y. Yamada, Y. Shibata, T. Okugawa, and K. Habara. *High-level fluctuation tolerant optical receiver for optical packet switch and WDM cross-connect*. Journal of Lightwave Technology, 16(12):2220–2227, Dec. 1998.

[13] Y. Akahori, T. Ohyama, M. Oguma, K. Kato, and Y. Yamada. *Hybrid integrated differential photoreceiver module for photonic packet switching systems using a planar lightwave circuit platform*. IEEE Photonics Technology Letters, 10(6):869–871, Jun. 1998.

[14] Y. Yamada, Y. Shibata, and K. Habara. *10 Gbit/s differential receiver for optical power fluctuation*. Electronics Letters, 33(19):1642–1644, Sept. 11 1997.

[15] Y. Yamada, M. Togashi, K. Habara, and T. Matsunaga. *Burst-mode differential receiver for optical packet communication*. Electronics Letters, 32(16):1500–1501, Aug. 1 1996.

[16] MAXIM. *10.7Gbps Linear Transimpedance Amplifier with Output Offset Adjust Datasheet*. `http:/www.maxim-ic.com/`.

[17] T. De Ridder, P. Ossieur, X. Yin, B. Baekelandt, C. Mélange, J. Bauwelinck, X. Z. Qiu, and J. Vandewege. *BiCMOS variable gain transimpedance amplifier for automotive applications*. Electronics Letters, 44(4):287–288, Feb. 14 2008.

[18] T. Vanisri and C. Toumazou. *Integrated High-Frequency Low-Noise Current-Mode Optical Transimpedance Preamplifiers - Theory and Practice*. IEEE Journal of Solid-State Circuits, 30(6):677–685, Jun. 1995.

[19] P. Ossieur, D. Verhulst, Y. Martens, W. Chen, J. Bauwelinck, X.Z. Qiu, and J. Vandewege. *A 1.25-Gb/s burst-mode receiver for GPON applications*. IEEE Journal of Solid-State Circuits, 40(5):1180–1189, May 2005.

[20] T. Nakanishi, Y. Fukada, K.-I. Suzuki, N. Yoshimoto, M. Nakamura, K. Kato, K. Nishimura, Y. Ohtomo, and M. Tsubokawa. *Wide dynamic range and high sensitivity APD burst receiver configuration based on /i M/-switching technique for 10 GEPON System*. In LEOS 2007. 20th Annual Meeting of the IEEE Lasers and Electro-Optics Society, pages 876–7, 2007 2007.

[21] S. Vatannia, P.H. Yeung, and C. Lu. *A fast response 155-Mb/s burst-mode optical receiver for PON*. IEEE Photonics Technology Letters, 17(5):1067–1069, May 2005.

[22] T. De Ridder, P. Ossieur, B. Baekelandt, C. Mélange, J. Bauwelinck, C. Ford, Xing-Zhi Qiu, and J. Vandewege. *A 2.7 V 9.8 Gb/s burst-mode TIA with*

fast automatic gain locking and coarse threshold extraction. In 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 220–1, 2008 2008.

[23] P. Ossieur, T. De Ridder, J. Bauwelinck, E. De Backer, J. Gillis, X. Z. Qiu, and J. Vandewege. *1.25 Gbit/s ITU-T G.984.2 burst-mode transimpedance amplifier without reset pins*. Electronics Letters, 43(18):991–993, Aug. 31 2007.

[24] S. Nishihara, S. Kimura, T. Yoshida, M. Nakamura, J. Terada, K. Nishimura, K. Kishine, K. Kato, Y. Ohtomo, N. Yoshimoto, T. Imai, and M. Tsubokawa. *A burst-mode 3R receiver for 10-Gbit/s PON systems with high sensitivity, wide dynamic range, and fast response*. Journal of Lightwave Technology, 26(1-4):99–107, Jan.-Feb. 2008. Conference on Optical Fiber Communications/National Fiber Optic Engineers Conference (OFC/NFOEC), Anaheim, CA, Mar., 2007.

[25] M. Nakamura, Y. Imai, Y. Umeda, J. Endo, and Y.J. Akatsu. *1.25-Gb/s burst-mode receiver ICs with quick response for PON systems*. IEEE Journal of Solid-State Circuits, 40(12):2680–2688, Dec. 2005. IEEE International Solid-State Circuits Conference (ISSCC 2005), San Francisco, CA, Feb. 06-10, 2005.

[26] P. Ossieur, X.Z. Qiu, J. Bauwelinck, and J. Vandewege. *Sensitivity penalty calculation for burst-mode receivers using avalanche photodiodes*. Journal of Lightwave Technology, 21(11):2565–2575, Nov. 2003.

[27] Q. Le, S.G. Lee, H.Y. Kang, and S.H. Chang. *A CMOS Burst-Mode TIA with Step AGC and Selective Internally Created Reset for 1.25Gb/s EPON*. In 2007 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, pages 50–51, Feb. 2007.

[28] M.R. Leadbetter, G. Lindgren, and H. Rootzén. *Extremes and related properties of random sequences and processes*. New York (N.Y.): Springer, 1983.

[29] *FastHenry*. `http://www.fastfieldsolvers.com/`.

[30] MAXIM. *MAX3971/MAX3971A Evaluation Kits Datasheet*. `http:/www.maxim-ic.com/`.

4

10 Gb/s Burst-Mode Post Amplifier

The PIEMAN BM-Rx consists of an integrated BM PIN-TIA module and a BM-PA chip located at the Optical Line Terminal (OLT). As described in Chapter 2 the functionality of the BM-Rx is more complex than that of a CW-Rx. The combined requirement of high sensitivity and a wide DR makes the 10G BM-Rx design very challenging. The PIEMAN BM-Rx is shown in Figure 4.1. The BM-PA follows

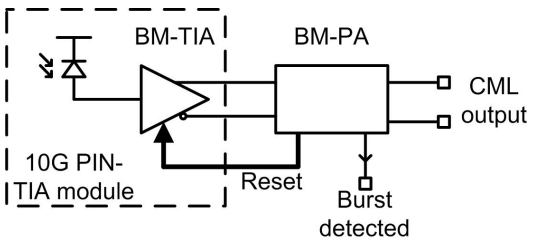

Figure 4.1: BM-Rx (inter)connections

the BM-TIA, takes the output voltage from the TIA and converts it into output signals with levels compatible with a standard logical format (in this case CML). The optical power budget specifications of the BM-Rx were chosen as similar as possible to those in GPON. After an investigation into possible topologies a multistage feedforward receiver scheme was chosen for PIEMAN.

The most advanced and important functionalities in BM-Rx's are automatic reset generation and burst detection. The reset signal serves to erase all memory like gain and threshold settings from a preceding burst, and prepare both the BM-

TIA and BM-PA for the next burst. This reset signal is given within the guard time. As shown in Figure 4.1 the reset generated by BM-PA is used by the BM-TIA. The burst detected signal is used by the BM-CDR. In this way the burst detection and automatic reset generation circuits simplify the interface between higher network layers and the physical layer. The designed reset block counts the time since the last received one. If this time exceeds the maximum length of CID (plus an extra delay for robustness) a reset signal is generated. This reset signal can then be used on the preceding TIA. The reset is also used on the BM-PA to reset all the PKDs until activity is detected again. This automatic reset generation circuitry is an advanced feature that has never been reported before on 10 G GPON-like Rx's [1]. A patent application was filed on this feature [2].

The advanced reset and burst detect circuits are highlighted in Section 4.1. The architecture study is given in Section 4.2. The BM-PA specifications are also included in this section. The BM penalty of the designed BM-PA is calculated in Section 4.3. Section 4.4 gives details of the top level architecture of the BM-PA. In Section 4.5 the important circuits are explained in detail. The reset and burst detection implementation details are respectively covered in Section 4.6 and 4.7. Layout, packaging and printed circuit board (PCB) are shown in Section 4.8 and this chapter concludes with the measurement results in Section 4.9.

4.1 Advanced Features of the BM-PA

4.1.1 Reset signalling

To ensure high traffic efficiency, short guard times (25.6 ns) between bursts and short preambles ($<$ 50 ns) are required. A reset signal is used to erase all information from the previous burst and prepare the Rx for the next burst. This reset signal usually originates from the MAC layer which knows arrival and end times of bursts from all ONUs. Omitting this reset greatly simplifies the interface between physical and MAC layer and enables the use of these BM-Rx's in reamplification, regeneration and retiming (3R) nodes where no such timing information is available. So it is a great benefit if the BM-Rx itself (so the physical layer) is capable of detecting when a new burst starts and especially when the burst ends as it is not always straightforward to apply a reset signal to the BM-TIA. E.g., considerations like cheap packages (TO-can for GPON) can make it impossible or very impractical to signal the end of burst to TIA and LA. When a limited number of pins are available, common-mode signalling as used in [3] and patented in [4] offers a solution. The reset signal still has to be given to the BM-PA, but this chip usually has a larger number of pins.

Two methods can be used to detect the end of a burst. Firstly, the lack of data transistions indicates the end of a burst. Secondly, the drop in input signal power

can be measured. In GPON the guard time is 25.6 ns and the longest string of CID is 72 bits, so 57.6 ns. If one wants to use the lack of transitions as a way to indicate the end of a burst, then the guard time should be longer than the CID. The BER should also be sufficiently low, so that the error of wrongly detecting the end of the burst, or missing the end of a burst remains sufficiently low. In GPON, it is obviously impossible to detect the end of the burst from the lack of signal transitions alone [5]. Using signal level detection is also difficult, as the Tx is not turned off immediately after the end of the burst so the zero level is detected for a while after the burst has ended. In GE-PON, where the guard times and preamble lengths are significantly larger, reset detection methods have been reported [6]. In the PIEMAN network, the guard time is longer than the CID time, so the automatic reset generation circuitry is based on measuring the time since the last received '1'.

4.1.2 Previous BM-Rx's without external reset

In [7] a 155 Mb/s resetless BM-Rx was presented. Feedback is used to set the threshold of the next bit depending on the previous bit and to avoid overloading the TIA. At 10 Gb/s it is very difficult to ensure stable high-speed feedback loops. Also, the system only functions well for an ER of exactly 10 dB which is difficult to maintain in a network. In [8], the envelope of the burst is detected and a reset is created when this envelope crosses a reference voltage close to the dc voltage of the Rx outputs. Due to the slow decay of the PKD used to detect the envelope of the burst, a guard time of at least 250 ns is required. The BM-Rx in [6] is ac-coupled and does not require any reset signal because no PKDs are used. However, the required guard time is still 100 ns. The automatic reset generation circuitry designed for the PIEMAN BM-Rx functions up to a minimum guard time of 25.6 ns.

4.1.3 Burst detection

The burst detection is a more commonly implemented feature in BM-Rx's. It is used to signal to the BM-CDR when valid logical levels are output. The BM-CDR can then start its clock phase extraction. In the PIEMAN 10 Gb/s BM-PA this burst detect signal is also used to align the internal PKD reset release signals (see Section 4.6) with the incoming data. In combination with the automatic reset generation this totally omits the need for time critical signalling from MAC to the BM-Rx.

4.2 Study of Offset Compensation and Decision Threshold Extraction Techniques

The specifications of the BM-PA are summarized in Table 4.1. One of the requirements within PIEMAN was a dual-rate operation of the BM-Rx. In that way, a fall-back solution to a bit rate of 5 Gb/s was foreseen in case the 10 Gb/s operation proved too challenging. The supply was again chosen to be higher than the typical operation voltage of the technology (i.e. 2.5 V) because the PKDs needed a larger head room to detect the peaks of the signals in the first stage. Based on the above specifications, one of the 4 BM-Rx approaches explained next was chosen. The 4 BM-Rx configurations are distinguished based on how the offset

Parameter	**Min.**	**Typ.**	**Max.**	**Remark**
Bit-rate (Gb/s)	5	10		
Bits used for PA (bits)	200		232	
Sensitivity (mV, differential)		20		@ 10 Gb/s, BER = 10^{-10}
Overload (mV, differential)		500		
Small signal 3 dB bandwidth (GHz)		8		
Pulse width distortion (%)		± 5	$\pm$ 10	
supply voltage (V)	2.6	2.65	2.7	
Ambient temperature (°C)	0	27	70	

Table 4.1: BM-PA specifications

is compensated and the threshold is extracted. The choice can be made between feedback [9, 10], feedforward [11, 12], a combination of both [13, 14], and delayed feedforward [15]. In the latter option, the offset and threshold information is measured during an 'offset measurement round' for each ONU and then stored at the OLT in a table. As the MAC layer at the OLT exactly knows the order in which the ONUs send bursts, it is possible to anticipate to the next burst by setting the threshold and offset compensation ready for that specific ONU. As this approach is not very practical in networks with a large number of ONUs, like the PIEMAN network, this architecture was not investigated.

4.2.1 BM-Rx with feedback loop

In a feedback BM-Rx, a feedback loop is closed around the Rx to remove the dc-offsets and extract the decision threshold. This feedback loop should be very fast to ensure fast extraction of the decision threshold but on the other hand, the speed of the feedback loop should be kept low enough to ensure stability. As the forward path has a pole at the bandwidth frequency of around 8 GHz, the dominant pole in the feedback loop should be placed at a much lower frequency to maintain

stability. This means that the settling of the loop will happen on a time scale that is long compared to the preamble specified in the PIEMAN system. Therefore, this approach was not used for the PIEMAN BM-Rx. Examples of a feedback BM-Rx's are given in [9, 10]. Figure 4.2 shows the Rx in [9]. A differential TIA

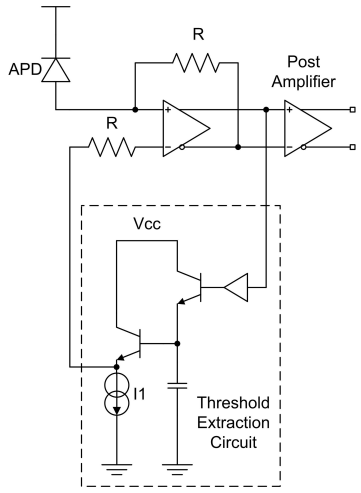

Figure 4.2: Offset compensation using feedback

is used, and the positive peak of the positive output is detected and fed back to the input. As this is the maximum of a differential signal, the fed back threshold will be halfway the differential signal swing. To implement this approach for PIEMAN would require a very fast PKD (almost within a bit). The PKD in the feedback loop should also be used in the gain determination because the signal swing after the preamplifier is changed by the feedback loop, so the signal strength cannot be determined at the same time. As explained in Section 4.5.1, the used technology did not allow for such fast PKDs to be implemented. The relatively slow PKDs would mean that the settling time would become too large.

4.2.2 BM-Rx combining feedback and feedforward

A second promising approach is the combination of feedback and feedforward taking the advantage of feedback with very accurate offset removal and the advantage of feedforward with very quick threshold extraction (THE) or offset measurement. In this way, the disadvantages of both approaches can be mitigated.

The Rx in [14] was designed by INTEC_design within the scope of the IWT funded project Sympathi (SYMmetrical PON AT High bit rate) as part of a PhD dissertation [16]. The THE circuits detect the positive and negative peaks of both signal phases and set the threshold halfway by use of a resistive divider. This

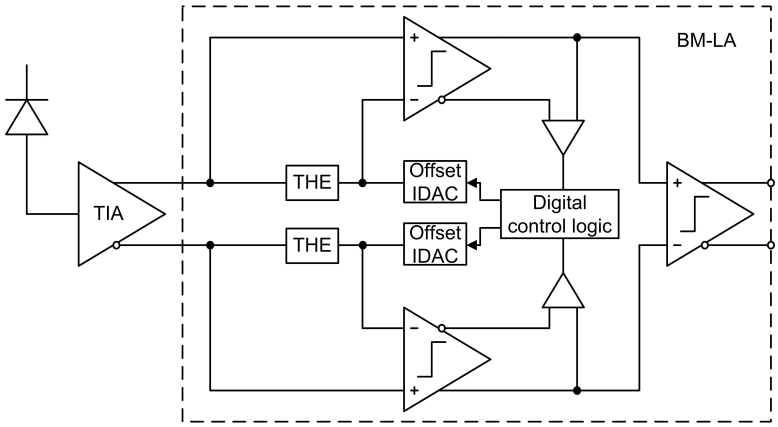

Figure 4.3: Rx architecture combining feedback and feedforward

threshold is fed to the first stage limiting amplifiers *LA1P* and *LA1N*. The positive outputs of these limiting amplifiers are then input to the second stage limiting amplifier *LA2*, which is the output buffer of the chip. Differential offsets of the TIA output are removed by the THE circuits. Any offsets of the PKDs and the first limiting stage amplifiers will cause a BM penalty (see Section 4.3). Therefore this offsets needs to be compensated. Any signal independent offset of the PKDs has similar effects as the offset of the limiting amplifier so ideal PKDs are assumed and only the offsets of *LA1P* and *LA1N* are considered. The offset was digitally compensated by a feedback loop that was only closed during dark periods, i.e. periods during which no light is sent upstream. Then, the differential output of the first stage limiting amplifiers is a measure of the offset of those amplifiers. The digital control logic sets the output currents of the current digital to analog converter (IDAC)s such that the amplified error voltage is zero. These currents create a voltage drop across the resistive bridge in the THE circuits that compensates for the offset of the limiting amplifiers. The offset of *LA2* is less important because the signal to offset ratio has already been increased by the first stage limiting amplifiers and hence the BM penalty will be small. The offset compensation loop needs to be closed regularly to track the change of the offset with temperature. Because temperature changes have a relatively large time constant a dark period frequency of 2 Hz is sufficient.

The use of a digital control loop was not possible within PIEMAN because of power consumption, die area and risk of crosstalk. Besides this, dark periods in a network with up to 512 ONUs would unnecessarily complicate the network protocol and reduce transmission efficiency. This architecture can be modified to suit the PIEMAN network specifications by storing the offset information on capacitors. The feedback loop should also be closed during bursts to avoid the

need for dark periods. The output signals of the limiting amplifier are given by

$$V_{LA} = V_{CM} \pm \frac{A}{2} V_{OS} \pm \frac{A}{2}(V_{IN,P} - V_{IN,N}) \quad (4.1)$$

$$V_{LA} = V_{MAX} \quad (4.2)$$

$$V_{LA} = V_{MIN}. \quad (4.3)$$

Where (4.1) is for small input signals with $A(V_{IN,P} - V_{IN,N}) < V_{MAX} - V_{MIN}$, and (4.2) and (4.3) are for larger input signals, respectively for positive and negative differential input signals. From these equations it is clear that the offset information disappears from the output signals when the signals are limited. This implies that the feedback loop should be opened before the input signals are limited. As it is not guarantueed that one of the ONUs will produce such a weak Rx input power that the signals are amplified linearly within the limiting amplifier, this implies that the offset compensation loop has to close, settle and open again within the minimum guard time of 25.6 ns. This is extremely short for the settling of a feedback loop. As explained before, stabilizing a feedback loop around a 10 Gb/s datapath that has to settle within less than 25.6 ns is very difficult. It would require fast PKDs with a signal independent offset. As will be shown in Section 4.5.1 the PKDs that can be implemented in the chosen technology are not extremely fast, not accurate and they have a signal dependent offset. Therefore this approach was not implemented for the PIEMAN project.

4.2.3 Multistage feedforward

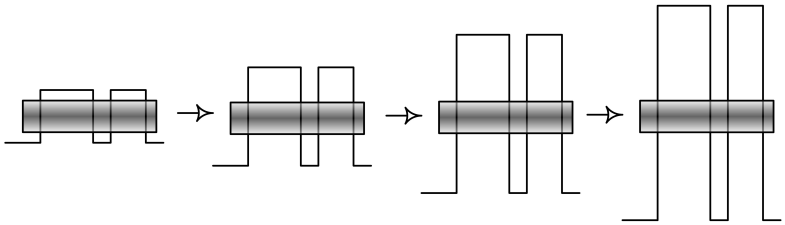

Figure 4.4: Multistage feedforward BM-Rx operation [17]

The third option is the multistage feedforward BM-Rx. This Rx measures and sets its decision threshold prior to amplifying. The offsets of amplifiers and PKDs are not removed however. The operation of this Rx relies on the fact that the signal to offset ratio increases with every amplifier stage thus gradually improving accuracy. In that way the effect of the offsets is mitigated and the BM penalty can effectively be reduced. This is illustrated in Figure 4.4 where the gray shaded areas indicate the amplifier offset, which is a random variable.

The advantage of this feedforward structure is the very fast THE. However, the disadvantage is the inaccurate offset removal and noisy threshold caused by this fast THE [18]. An example of a BM-Rx using this technique is given in [11]. As the other BM-Rx's did not meet the specifications of the PIEMAN project, this multistage feedforward architecture was chosen. The number of stages will be determined in Section 4.3.2. As long as the required preamble is a valid 5 Gb/s signal the dual-rate specification is easily met by this architecture.

4.3 Burst-mode Penalty

The BM-PA's task is removing offsets and amplifying the input signals to logical levels. The BM-PA will incur a BM penalty (compared to a limiting amplifier working in continuous mode) [18–21]. This penalty has different causes:

1. Fast acquisition of the noisy threshold will give rise to a threshold that effectively varies from burst to burst, even if this burst has the same optical power. This gives rise to a BM penalty ranging from 0.5 dB to 2 dB, depending upon the details of the THE implementation.

2. The BM-PA is dc-coupled, hence any dc-offset in the signal path will give rise to a sensitivity penalty.

3. The incoming burst may show slow tails, which could impair the operation of the THE circuitry.

4. The finite gain of the BM-PA gives rise to an additional sensitivity penalty. This is true whether the Rx operates in BM or in CW. Indeed, every amplifier has a finite gain. At the output of the BM-PA, the levels need to be compatible with CML logical levels, which signify the sensitivity of the CDR input. Hence, levels at the input of the BM-PA that do not get amplified above this sensitivity level will give rise to bit errors. A sensitivity penalty is therefore incurred, which becomes smaller with increasing PA gain.

4.3.1 Theoretical BER calculations in case of multistage feedforward Rx

Assume that the input noise is Gaussian with average signal level μ_{in} and standard deviation σ_{in}. If this noisy signal is amplified by an ideal linear amplifier, the noise at the output is again Gaussian, but now with average $A\mu_{in}$ and deviation $A\sigma_{in}$ [22].

Figure 4.5a shows the situation for an ideal linear amplifier. The limiting amplifier's clipping functionality will also clip the noise distribution. (see 4.5b). The Gaussian distribution will lose its tail (above clipping level) and the chance that

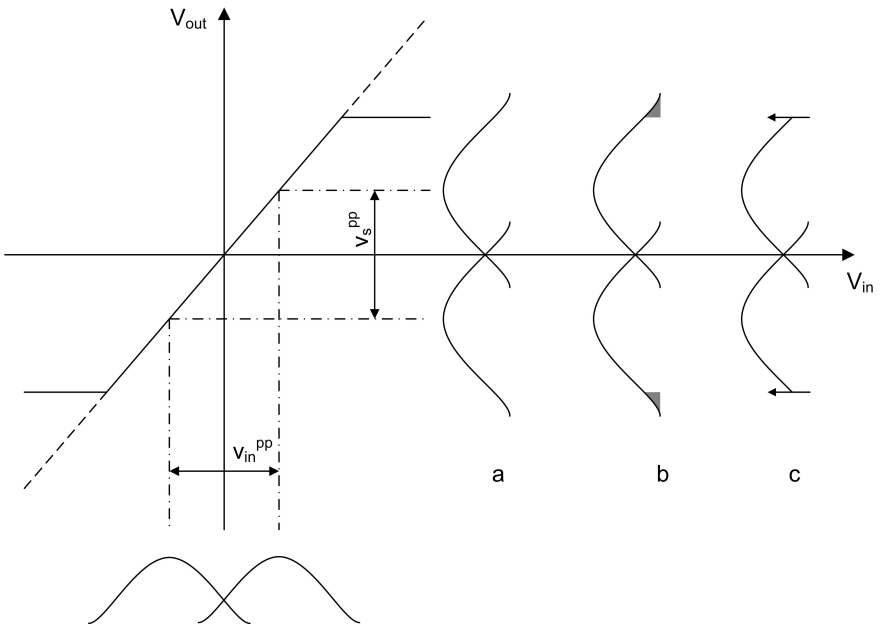

Figure 4.5: Burst-mode penalty illustration

V_{out} equals $V_{out,max}$ is equal to the grey area in 4.5b. The remaining distribution will look like the distributions in Figure 4.5c. In case of Gaussian noise on the ones and the zeros, the bit-error-ratio is given by the area under the Gaussian tails (see Figure 2.4 in section 2.1.4). This part is not clipped, and the clipped part is transformed into a Dirac-impuls with value equal to the chance the signal is clipped. So considering the exact distribution of the clipped tail is irrelevant for the tail used to calculate the BER and we will calculate the BER as if the limiting amplifier was a linear amplifier. The BER can thus be calculated by the well-known formula (2.11) with

$$Q = \frac{v_s^{pp}}{2A\sigma}. \tag{4.4}$$

Note that v_s^{pp} is not the maximum clipped output swing. It is the distance between the averages of the noise distributions in case there would be no clipping. This means

$$v_s^{pp} = Av_{in}^{pp}. \tag{4.5}$$

It is now clear that for BER-calculations one can pretend that all noise distributions are Gaussian as if no clipping is present (note that it is assumed the noise on one and zero level is indeed Gaussian and both have the same distribution). In case of an ideal amplifier (no offsets and infinite sensitivity of decision circuit) the BER isn't improved by using more stages, as can be seen from formula (4.4) and (4.5).

The above conclusions are valid in case of a DEC with infinite sensitivity. In case of a DEC with sensitivity V_{DTA}, the BER is given by Equation (4.7).

$$BER = \int_{-\infty}^{-\frac{V_{DTA}}{2}} f_Y(y)dy \tag{4.6}$$

$$= \frac{1}{2}\operatorname{erfc}\left(\frac{Q}{\sqrt{2}}\right) \tag{4.7}$$

$$Q = \frac{v_s^{pp}}{2A\sigma} - \frac{V_{DTA}}{2A\sigma}. \tag{4.8}$$

There are more errors in case of finite DEC sensitivity because the chance of a bit error is now the chance a '1' is lower than VDTA/2 instead of '0' previously. By substituting (4.5) in (4.8) one can see that the first term in Equation (4.8) remains the same despite increasing the total gain by using more stages. The second term decreases with increasing gain A, so Q increases as the gain increases and the BER decreases with increasing (total) gain.

$$BER = \frac{1}{2}\left(\int_{-\infty}^{0} f_{Y_1}(y)dy + \int_{0}^{\infty} f_{Y_0}(y)dy\right) \tag{4.9}$$

$$= \frac{1}{4}\left(\operatorname{erfc}\left(\frac{Q_1}{\sqrt{2}}\right) + \operatorname{erfc}\left(\frac{Q_0}{\sqrt{2}}\right)\right) \tag{4.10}$$

$$Q_1 = \frac{v_s^{pp}}{2A\sigma} - \frac{V_{os}}{\sigma} \tag{4.11}$$

$$Q_0 = \frac{v_s^{pp}}{2A\sigma} + \frac{V_{os}}{\sigma}. \tag{4.12}$$

In case of n gain stages Equation (4.11) and Equation (4.12) are given by

$$Q_1 = \frac{v_{in}^{pp}}{2\sigma} - \frac{V_{os}}{A^{n-1}\sigma} \tag{4.13}$$

$$Q_0 = \frac{v_{in}^{pp}}{2\sigma} + \frac{V_{os}}{A^{n-1}\sigma}. \tag{4.14}$$

It is clear that, the more total gain (or the more stages), the less the effect of the offset.

The BER in case of a finite DEC sensitivity and offset can be calculated with formula 4.10 by replacing v_s^{pp} with $(v_s^{pp} - V_{DTA})$.

The transfer function of the limiting amplifier was approximated by a linear approximation. In reality this transfer function is a $\tanh(V_{in})$. $\tanh(x)$ is well approximated by a linear curve for small values of x, but not for larger values. So for small values the resulting tail of the noise distribution would still be Gaussian; however for larger values, this would not be the case. For the BER calculation however, only the tail that is transformed by the linear part of $\tanh(x)$ is used. This justifies the use of the linear approximation of the transfer function.

We now have formulas to directly calculate the BER in function of the SNR at the first stage, the offset and the DEC sensitivity. Note that the maximum output voltage is not in these equations. However it is important that this maximum output voltage is large to make the maximum allowable offset large enough (otherwise BER is about 0.5). We can now calculate the BER for different gain and offset and SNR.

4.3.2 Dimensioning the multistage feedforward approach

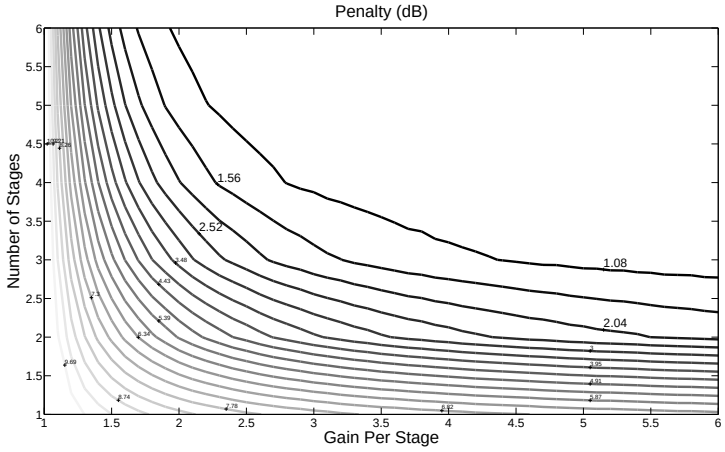

Figure 4.6: BM penalty contourplot for 4 THE stages

Using Equations (4.15)-(4.17) the BER was calculated for a multistage feedforward amplifier with n stages and gain A per stage. The expressions were modified to account for the different noise distributions on the '1' and '0'.

$$Q_1 = \frac{V_{in}^{pp}}{(2\sigma_1)} - \frac{V_{DTA}}{2A^n\sigma_1} - \frac{V_{os}}{A^{n-1}\sigma_1} \tag{4.15}$$

$$Q_0 = \frac{V_{in}^{pp}}{(2\sigma_0)} - \frac{V_{DTA}}{2A^n\sigma_0} + \frac{V_{os}}{A^{n-1}\sigma_0} \tag{4.16}$$

$$BER = 0.25 \cdot \left(\operatorname{erfc}\left(\frac{Q_1}{\sqrt{2}}\right) + \operatorname{erfc}\left(\frac{Q_0}{\sqrt{2}}\right)\right). \tag{4.17}$$

The input signal swing required for a BER of 10^{-10} was compared to the input signal swing required for the same BER but in a Rx without offsets and with infinite DEC sensitivity. This gives the penalty of the multistage feedforward architecture. This penalty was calculated for a total offset of 50 mV. This does not mean that the differential offset of the input signals is limited to 50 mV. The offset in these

equations is the error on the ideal threshold and this error is caused by combined contributions of amplifier input offset and inaccuracy of the PKDs and THE circuitry. V_{DTA} was chosen 200 mV. This specification is based on the CML-input signal requirement of the CDR.

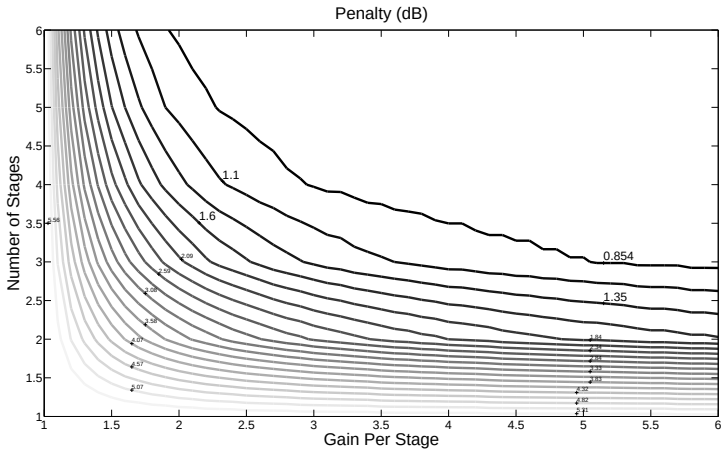

Figure 4.7: BM penalty contourplot for 4 THE stages and extra gain stage

Figure 4.6 shows a contourplot of the penalty for a different gain per stage and a different number of stages. A 3.5 dB penalty due to a slicing factor of 0.5 (see Section 4.4.2) was substracted to evaluate the penalty caused by the architecture choice itself. The goal is to achieve a penalty lower than 1 dB. The total penalty still exceeds the 4 dB penalty specification of the BM-Rx. However, a multistage feedforward penalty smaller than 1 dB would consume too much power and die area. As can be seen in Figure 4.6, with only a little bit of gain, a large number of stages would be needed to limit the penalty. With a small amount of stages, more gain per stage is needed. For a penalty lower than 1 dB, about 3 stages are needed with a gain of over 4. The achievable gain per stage is not infinite if the bandwidth specification also has to be met. Therefore, it was investigated whether the gain and the penalty could be reduced by first using a number of stages with low gain per stage to remove the penalty caused by the offset to then remove the penalty caused by the finite DEC sensitivity by using an additional amplifier with high gain without THE. The output buffer is such a gain stage without THE so no additional circuit is needed. Equations (4.15) and (4.16) were modified to (4.18) and (4.19) to include the output buffer gain. The result for an output buffer gain of 16 is given in Figure 4.7. With 3 stages, now only a gain per stage of 3.5 is needed to limit the penalty to 1 dB. Another option is 4 stages with a gain per stage of

about 2.5. This option was chosen and implemented.

$$Q_1 = \frac{V_{in}^{pp}}{(2\sigma_1)} - \frac{V_{DTA}}{2A_e A^n \sigma_1} - \frac{V_{os}}{A^{n-1}\sigma_1} \tag{4.18}$$

$$Q_0 = \frac{V_{in}^{pp}}{(2\sigma_0)} - \frac{V_{DTA}}{2A_e A^n \sigma_0} + \frac{V_{os}}{A^{n-1}\sigma_0}. \tag{4.19}$$

In this way the BM penalty remains sufficiently small. This architecture requires that the gain in each stage is not so large as to actually drive the amplifier into limiting mode (for small signals with large offset). Therefore it was chosen to amplify the signals in the first 4 stages to signal levels larger than CML-levels. In this way the sensitivity penalty due to offsets can be reduced. The output buffer was used to increase the total gain of the limiting amplifier and to limit the signals to CML-output levels.

4.4 Chip Architecture of BM-PA

4.4.1 Top level architecture and building blocks

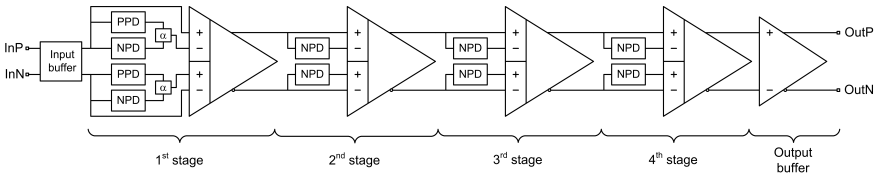

Figure 4.8: Post-amplifier data path

Figure 4.8 shows the datapath of the PA. It consists of an input buffer followed by 4 amplifier stages including THE and an output buffer. Besides the data path, advanced functionality is present: circuitry to detect the beginning of the burst and circuitry to detect the end of the burst (automatic reset generation). Circuits to generate voltage references and current references, and test circuitry are also included. NPD stands for 'negative PKD'.

The THE in the first stage consists of a traditional THE circuit similar to the one used in [14]: for every phase, both positive and negative peaks are extracted and a resistive divider sets the threshold halfway between both peaks. The next stages of the multistage feedforward achitecture use only negative PKDs to remove the offset. This is explained in Section 4.4.2. The use of only negative PKDs has implications on the slicing factor. In Section 4.4.2 it is shown that using only one type of PKDs inherently means that the threshold will be located halfway the eye opening.

4.4.2 Threshold scaling

As shown in Figure 4.8, only the first stage uses both positive and negative PKDs. The scaling factor can be chosen different from 0.5 by changing the resistive divider bridge. The positive PKDs in this THE block are inherently slower than their negative counterparts, so they determine the required preamble per stage. The PKDs in the first stage were designed to acquire their peaks rather slowly to improve accuracy as the input signals to the limiting amplifier can still be quite small. The result is that the first stage requires 7.0 ns to set its threshold. With 4 stages this would amount to a total preamble for the BM-PA of 28 ns. This leads to 34 ns combined with the 6 ns TIA preamble, which is outside the specified preamble length.

The comparators that are used in the PKDs need to be fast to limit the PKD error. This fast response requires large current consumption. The power consumption of the 4 PKDs in the first stage is 60 mW. With 4 stages this leads to 240 mW. The maximum power consumption of the Micro Lead Frame (MLF) package with 32 leads for 50 °C ambient temperature and 85 °C junction temperature is 1 W [23]. So 4 equal THE stages would consume 24 % of the total allowed power consumption.

So to limit power consumption and reduce the preamble length, the second, third and fourth stages only use negative PKDs to extract the thresholds of both phases [24]. How these two negative peaks can lead to a correct threshold setting will be explained in the next paragraphs.

The 10 Gb/s BM-TIA was described in Chapter 3. As the BM-TIA extracts a coarse threshold the signals at the input of the BM-PA will look like illustrated in Figure 4.9 instead of the signals in Figure 2.3 in Chapter 2. The positive and negative input signals are noted with V_P respectively V_N and their corresponding burst averages with V_{avgP} and V_{avgN}. V_{cm} is the common-mode level of the signals at the input of the BM-PA. While V_{cm} is the same for every burst, the signal amplitude V_S and the differential offset V_{os} will differ from burst to burst. As shown in Figure 4.9, the difference between both negative peaks $V_{PK,N}$ and $V_{PK,P}$ is equal to the differential offset V_{os} on the signal. This can also be shown mathematically. The positive phase V_P and the negative phase V_N can be written as

$$V_P = V_{cm} + (-1)^{1-b}\frac{V_S}{2} + \frac{V_{os}}{2} \tag{4.20}$$

$$V_N = V_{cm} - (-1)^{1-b}\frac{V_S}{2} - \frac{V_{os}}{2} \tag{4.21}$$

where b is the bit value, 0 or 1. The negative peaks $V_{PK,P}$ and $V_{PK,N}$ of respec-

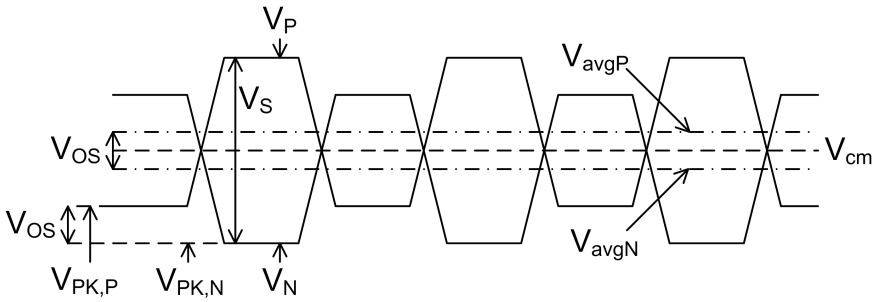

Figure 4.9: Offset illustration

tively V_P and V_N are given by

$$V_{PK,P} = V_{cm} - \frac{V_S}{2} + \frac{V_{os}}{2} \tag{4.22}$$

$$V_{PK,N} = V_{cm} - \frac{V_S}{2} - \frac{V_{os}}{2} \tag{4.23}$$

(4.22)-(4.23) gives

$$V_{PK,P} - V_{PK,N} = V_{os}. \tag{4.24}$$

Equation (4.24) shows that the offset can indeed be measured by using two negative PKDs. The ideal thresholds are given by

$$V_{TH,P} = \alpha V_{max,P} + (1-\alpha)V_{min,P} \tag{4.25}$$

$$V_{TH,N} = \alpha V_{min,N} + (1-\alpha)V_{max,N}. \tag{4.26}$$

α is the slicing factor, so 0.5 for equal noise distributions on zero and one, and less than 0.5 for unequal noise distributions. In the first stage, these thresholds are indeed calculated by acquiring both positive and negative peaks of both signal phases. The difference between those thresholds is given by

$$\Delta TH = V_{TH,P} - V_{TH,N} = (2\alpha - 1)V_S + V_{os}. \tag{4.27}$$

For $\alpha = 0.5$ this leads to V_{os}. This means that by extracting only the negative peaks of the threshold and applying V_{os} to the differential difference limiting amplifier (DDLA), we inherently apply a threshold with slicing factor 0.5. For $\alpha \neq 0.5$ knowledge of the signal swing is also needed and this knowledge is not comprised within the difference of the two negative peaks. The signal swing knowledge is comprised within the difference between common-mode level and negative peak. However, using V_{cm} leads to a very complex solution that could not be implemented in analog circuits. For these reasons, the threshold was put at 0.5. The BM penalty incurred by this is 3.5 dB and should be added to the penalty

calculated in Section 4.3. This is quite a large penalty, but it cannot be avoided given the power constraints of the package and the limitations of the used technology. As the latter stages implement a slicing factor of 0.5, the first stage was also designed to operate with a slicing factor of 0.5 to avoid pulse width distortion.

4.4.3 Input buffer

The input buffer of the PA provides a 50 Ω input impedance for the output buffer of the BM-TIA. In this way good high frequency matching is provided. The output buffer of the TIA was simulated together with the input buffer of the PA, including output bond wires of the TIA, and the complete package of the PA. The simulated input return loss is shown in Figure 4.10. Both common-mode and differential-mode input return loss remain below -10 dB up to 10 GHz.

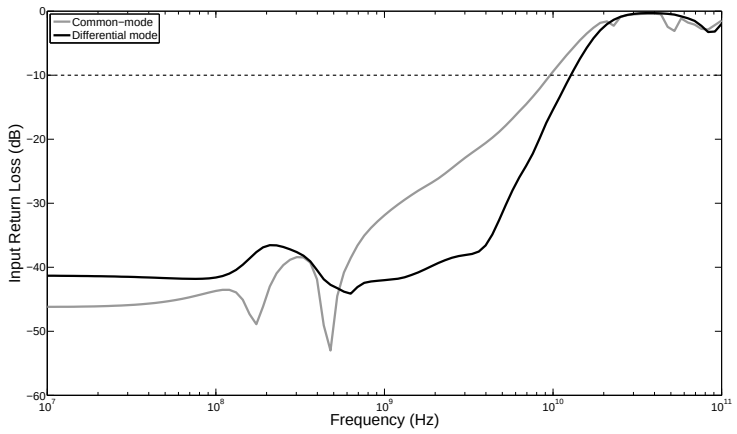

Figure 4.10: Simulated input return loss

4.5 Circuit Design of 10 Gb/s BM-PA

4.5.1 Peak detector circuit details

The required small response time implies that the PKDs used in the gain switching and on the PA have to acquire their peaks very quickly. In a multistage feedforward system, the threshold of the previous stage must have settled before the PKDs of the next stage can start acquiring their peaks. Considering the 4 stages in the multistage feedforward PA, each stage roughly has only one fourth of the total limiting amplifier response time to react. Traditional PKDs like the one in Figure 4.11 react to an input peak quickly and accurately because of the feedback loop.

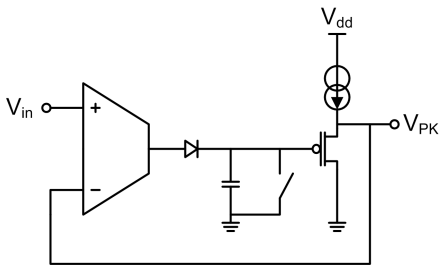

Figure 4.11: Positive PKD circuit using operational transconductance amplifier

The speed is limited by the settling time of the feedback loop and its stability. The accuracy is mainly limited by the loop gain and feed-through of input signals through the reverse biased diode once the peak has been acquired. Figure 4.11 shows an operational transconductance amplifier (OTA) which drives a diode and charges a capacitor as long as V_{PK} is lower than V_{in}. Without special measures, the OTA output stage will go out of its linear region (e.g. during reset as the output of the OTA is shorted to ground) meaning that it will react more slowly to the new peak that needs to be acquired. Extra diodes can be added to avoid this saturation. However, these measures require a supply voltage larger than $3V_{be}$ [25]. As V_{be} can become 0.9 V over temperature it is difficult to implement this PKD with the original 2.5 V supply. Besides this, the used SiGe technology does not allow HBTs in diode configuration because of current gain degradation during reverse emitter-base bias conditions [26]. This is because the extra carbon doping of the high-speed HBTs makes them very susceptible to current gain degradation. This means that, after several times of reverse biasing the diode connected HBT, the forward current gain will go down. For this reason, the circuit shown in Figure 4.12 was used for the negative PKDs on the TIA. The diode acting as a current switch has been replaced with a differential pair steered by a comparator. To allow a detected peak voltage range suitable for the limiting amplifiers, an extra follower was added in between transistor $M1$ and $M2$ and V_1 and V_{peak} respectively to implement the negative PKDs on the BM-PA (NPD in Figure 4.8).

4.5.2 Peak detector operation

To explain the peak detector operation we will first consider the circuit in Figure 4.12 without resistor R_H and without the input filter consisting of R_F and C_F. When the PKD is released after a reset (so when V_{Reset} becomes high), V_1 will be higher than V_{in} and the comparator will steer current I_{charge} completely through transistor Q_2 and hold capacitor C_H. This will charge C_H and V_1 will go down. When V_1 crosses V_{in}, the comparator will steer the charge current to the supply rail and the charge capacitor will hold the acquired peak level until a reset is given

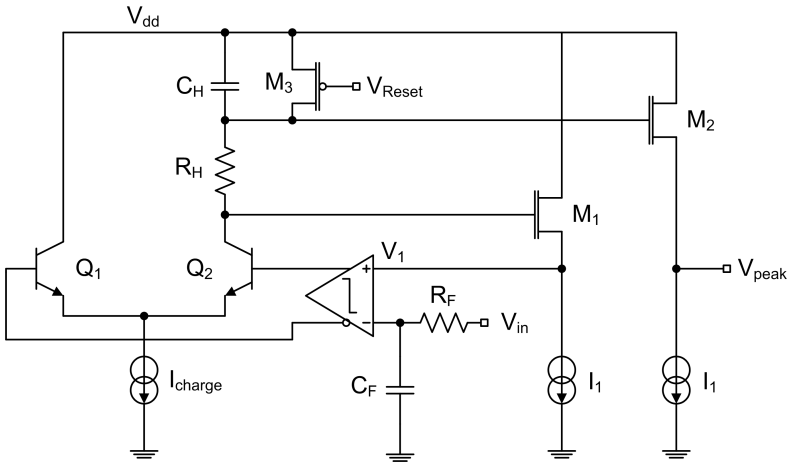

Figure 4.12: Negative PKD circuit

to the PKD. Because the comparator cannot instantly switch the current from Q_2 to Q_1 an error will be incurred (see Figure 4.13).

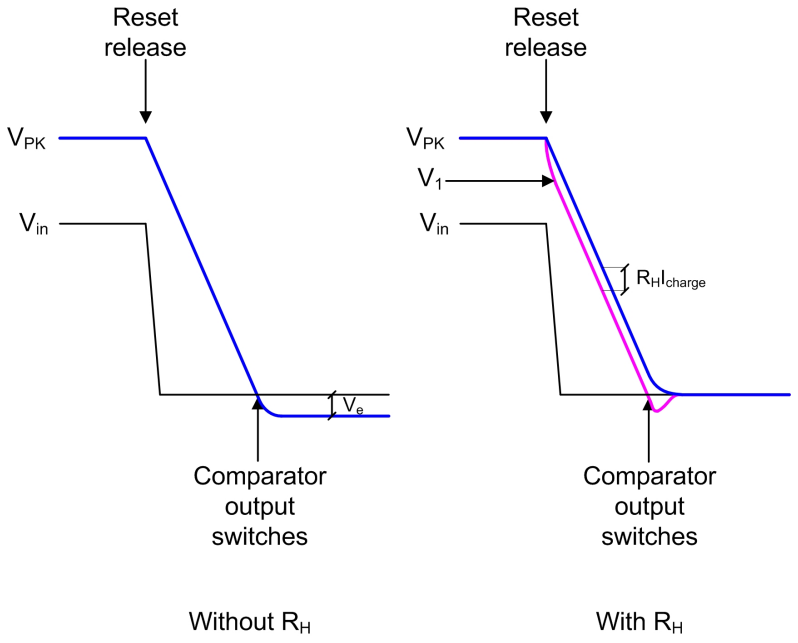

Figure 4.13: Outputs of negative PKD

The charging of the capacitor occurs with constant slope S_C given by equation

(4.28), so the speed of the PKD is in first order determined by the charge current and the hold capacitor.

$$S_C = \frac{I_{charge}}{C_H} \tag{4.28}$$

The higher the current, the faster the acquisition of the peak. Smaller capacitors yield faster PKDs; however, the minimum value for C_H is set by the stray capacitances. The PKD comparator can never end up in minimum overdrive condition because as long as the comparator is not toggled, V_1 will decrease with the constant slope S_C.

If the comparator has a delay δt this leads to an error V_e on the acquired peak level:

$$V_e = \frac{I_{charge}}{C_H}\delta t. \tag{4.29}$$

If a resistor R_H is placed in series with C_H, the comparator will switch before V_{peak} has reached the minimum level of input signal V_{in}. The current is already steered to the supply rail before V_1 reaches the peak level and $V_{peak} = V_{in}$ so R_H reduces the error. The error is completely removed when the voltage drop across R_H is equal to V_e. This leads to a value for R_H

$$R_H = \frac{\delta t}{C_H}. \tag{4.30}$$

Because the current decreases gradually during switching, R_H needs to be smaller than (4.30). Also, oscillations will occur if the resistor value is chosen to exactly compensate for the error or too large. A too small value for R_H on the other hand will have no effect. The replica structure M1-M2 reduces the feed-through

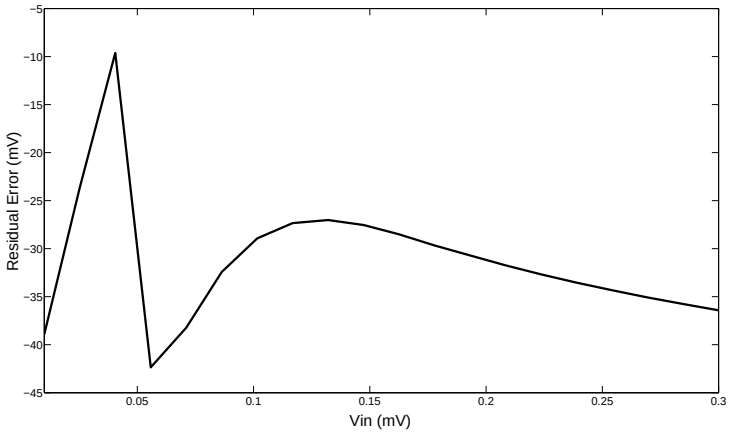

Figure 4.14: Residual error of negative PKD

from V_{in} towards V_{PK} after the peak has been acquired. The current I_{charge} was chosen as a compromise between speed and power consumption. Finally, the filter at the input filters out ringing peaks or overshoot on the input voltage for the PKD. Without the filter, the PKD would acquire these ringing peaks instead of the real peak value of the input signal.

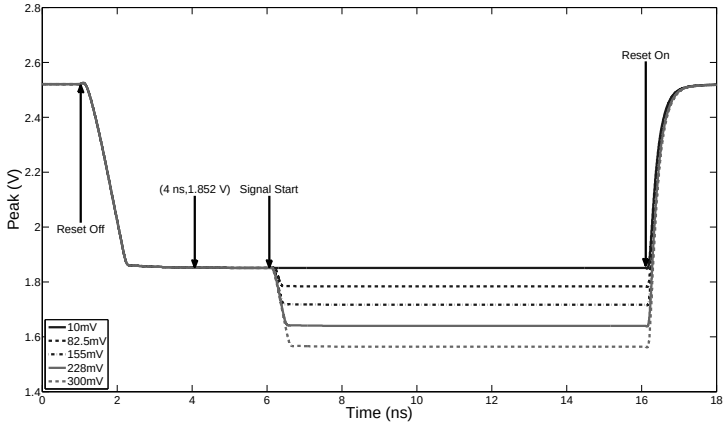

Figure 4.15: Negative PKD waveforms

There will always be a small remaining error on the detected peak. In the gain locking mechanism (see Section 3.4.3) this error can be compensated by changing the reference value. For the THE on the TIA this error is compenpensated by sending a small input current to the TIA generating the dark level reference. Another way to compensate for this error is to detect the dark level voltage with an identical PKD, but this consumes more power and die area.

However the offsets cannot be compensated for the detection of the peak levels of the input signals of the limiting amplifier. When using a positive and negative PKD, the offsets will more or less cancel out. Unfortunately, the positive PKDs have a larger error, because the current switch is made up from PNPs which are inherently slower. To add to the problem, the offset is signal dependent as shown in Figure 4.14. Different minimum signal levels were detected in simulation yielding Figure 4.14. The resulting detected peaks are given in Figure 4.15, where signal swing V_{in} was varied from 10 mV to 300 mV. For very small V_{in}, the output peak is already below the '1' level. Therefore the PKD does not react on the signal drop over V_{in} for these small input signals. This explains the decrease in error from 10 mV to about 40 mV. With $V_{in} > 40$ mV the PKD 'sees' the signal drop, acquires the new peak and ends up with a residual error of about 40 mV, which is required to avoid oscillations.

The positive PKD circuit is illustrated in Figure 4.16

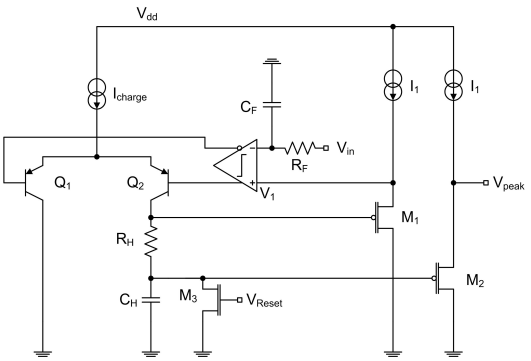

Figure 4.16: Positive PKD circuit

4.5.3 Amplifier stages

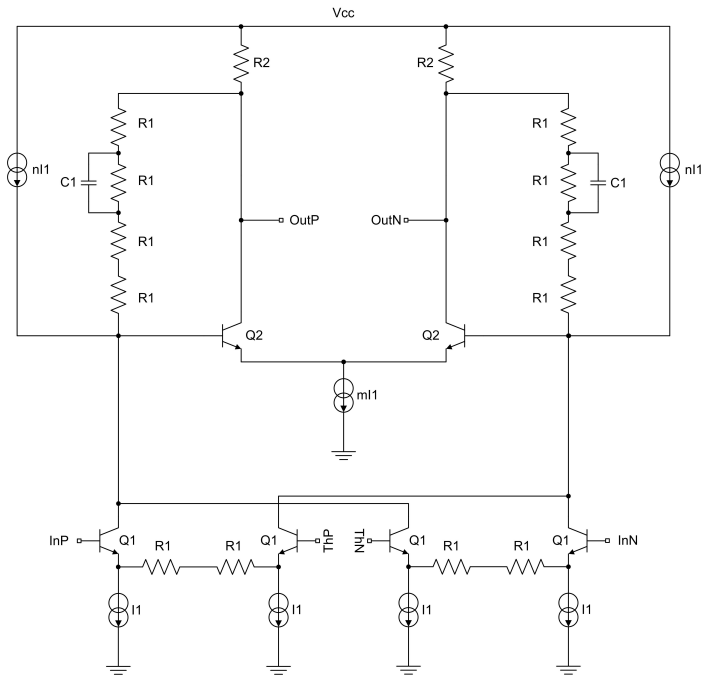

Figure 4.17: Limiting Amplifier circuit

Each stage uses the same limiting amplifier circuit shown in Figure 4.17. It is a DDLA with a Cherry Hooper architecture with emitter degeneration in the

transadmittance stage to reduce the gain, followed by a NPN buffer. These NPN followers are not shown in this figure. To shift the levels back to a common-mode level that can be detected by the next stage PKDs and limiting amplifier, the NPN buffers are followed by PNP level shifters. The need for a PNP level shifter after each NPN follower comes mainly from the limited supply voltage and leads to a larger power consumption because of all the extra PNP level shifters. Dc currents $n \cdot I1$ were added to the inputs of the transimpedance stage to avoid transistor saturation for larger signals. m was chosen 11 and n 10/3. Capacitor $C1$ was added to decrease the gain for high frequencies and thus improve the transfer characteristic. The DDLA limits the signals to a differential swing of 800 mV.

In the first stage, the positive and negative peak of both phases is acquired and a threshold is extracted for both positive and negative signal phase using resistive dividers. The outputs of the PKDs are input to a buffer (two level shifters in Figure 4.18). The outputs of this buffer is filtered by a resistive divider and capacitance C_1. The resistive divider sets the threshold slicing factor. A feedback loop is used to ensure that base-emitter drop of NPN and PNP is the same over all process corners and temperature. This feedback loop is shown in Figure 4.19. The feedback loop sets $V_{control}$ such that both inputs of the OTA are equal to V_{ref}. Since V_{ref} is also input to the base of $Q1$, this means that the base-emitter voltage drop of $Q1$ and $Q3$ will be the same.

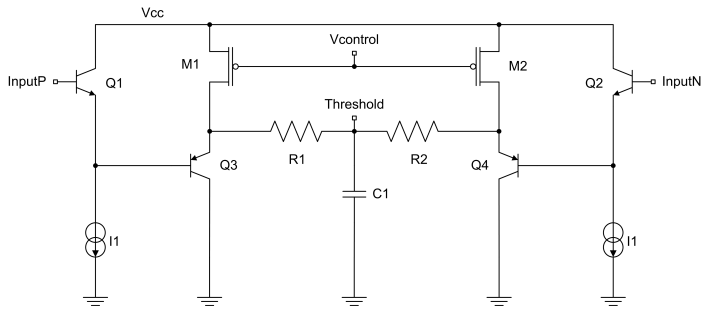

Figure 4.18: Threshold extraction circuit

4.5.4 Threshold extraction stage 2, 3 and 4

Figure 4.20 shows the second, third and fourth stages of the multistage feedforward amplifier. As explained before, these next three stages only use negative PKDs for offset compensation. For the largest signals the negative peaks will be outside the linear input range of the DDLA. So, directly feeding the negative peaks to the inputs of the DDLA can cause malfunction of the DDLA in case of very strong bursts. Another option is to input the detected peaks to one differential pair while

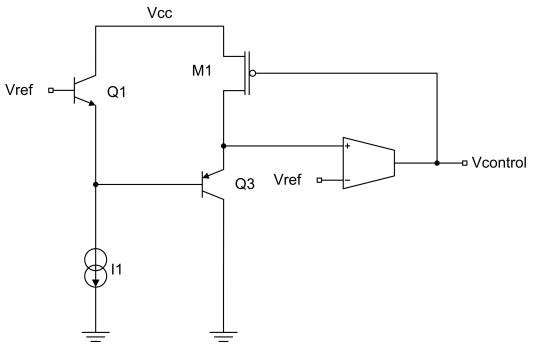

Figure 4.19: Feedback loop used in threshold extraction circuit

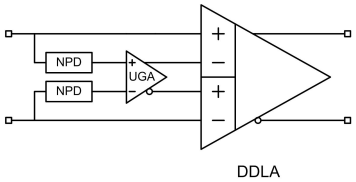

Figure 4.20: Threshold extraction based on negative peak detection only

the other differential pair amplifies both data signals. This can lead to one-sided limiting of signals, which is also unwanted. Therefore, the two negative peaks are shifted up to approximately the output common-mode level of the DDLA itself to ensure correct operation of the DDLA.

For this level shifting operation, a unity gain amplifier (UGA) is used. This is an amplifier with similar structure as the DDLA but with gain approximately equal to 1. The simulated gain is shown in Figure 4.21 over process corners and mismatch for the worst case temperature (in this case 0 °C) for 500 Monte Carlo runs. The average gain is 982 and the standard deviation is 12.2. This UGA superposes the difference between the detected negative peaks of both phases on the common-mode output voltage of the UGA. Due to the similar structure of the UGA and the limiting amplifier, this common-mode output voltage will be close to the common-mode output voltage of the limiting amplifier. Note that small differences in common-mode output voltage don't matter because of the differential difference architecture of the limiting amplifier.

Figure 4.22 shows the simulated offset of the DDLA for 85 °C for 200 Monte Carlo runs. The average offset is -386 μV and the standard deviation is 4.7 mV. This means that 66 % of the devices will have an offset smaller than 14.1 mV, which is well below the 50 mV offset specification used in the BM penalty calculations. This leaves sufficient room for the offsets caused by the inaccuracy of the

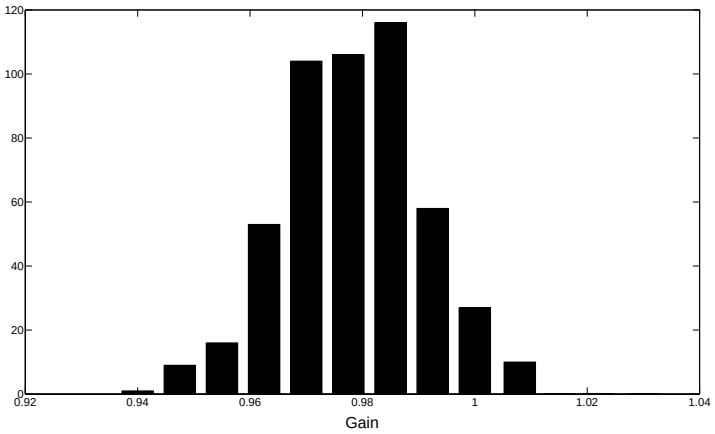

Figure 4.21: Gain over corners and mismatch for UGA

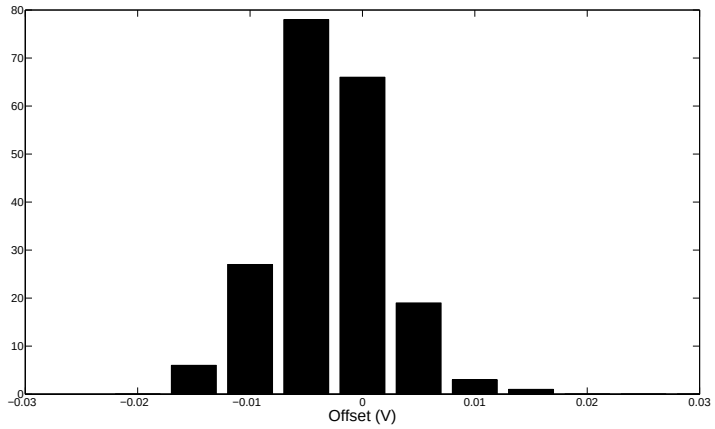

Figure 4.22: Offset of DDLA at 85 °C

PKDs.

A common-mode feedback loop would have simplified the system because then the output common-mode level of the DDLAs is known. However, due to the quick variations of the input common-mode from burst to burst and capacitive coupling, the common-mode feedback loop would set the common-mode to a different level than the actual common-mode level. Therefore it was chosen not to implement a common-mode feedback loop.

4.6 Automatic Reset Generation Implementation

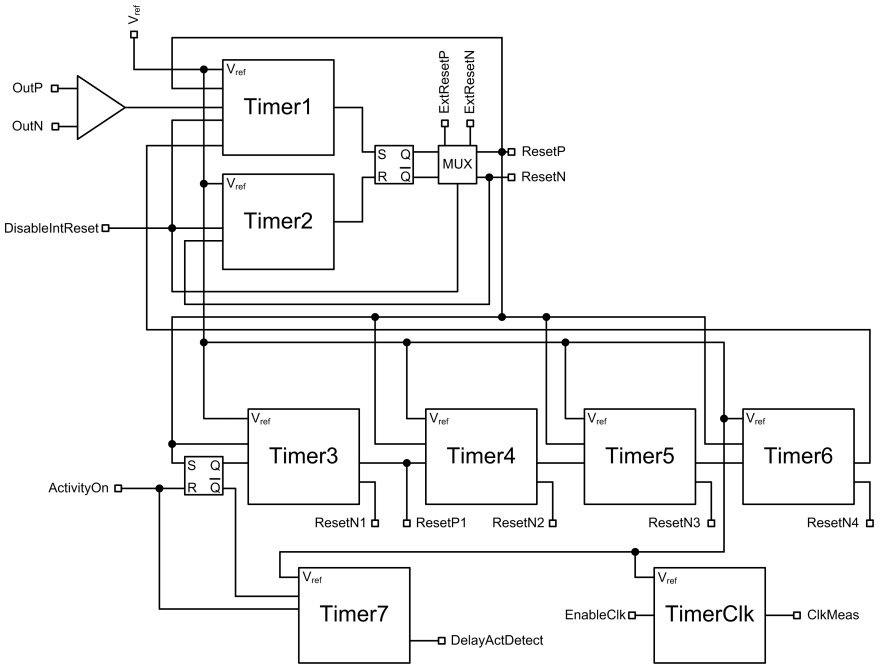

Figure 4.23: Top level of reset block

Figure 4.23 shows the top level architecture of the automatic reset generation circuitry. The squares are the inputs and outputs to the automatic reset generation circuitry. Table 4.2 summarizes these I/Os and their function. The reset block consists of 7 timers and a clock generation block for trimming, which also includes 2 timers and some logic. The inputs of the reset block are the outputs of the datapath. These outputs are amplified with a fast comparator and converted into CMOS signals. Every timer has one input for a reference voltage and a number of inputs to reset the timer. This will be explained in more detail in section 4.6.1. Timer1 and Timer2 are used for the detection of the end of a burst. Timer3, Timer4, Timer5 and Timer6 are used to delay the reset signals ResetP and ResetN for the different stages because the PKDs cannot be released before the previous threshold has settled. Timer7 is used to delay the start of the activity detection after a reset is detected so the system would keep generating resets until the next burst starts, which is unwanted. This is necessary because the outputs of the TIA will change when the reset has ended due to the TIA PKDs being released. Without delaying the activity detect one would possibly detect a reset immediately after the release of the reset. A multiplexer is used to choose between the internally created reset

Name	I/O	type	remark
V_{ref}	I	analog DC voltage	reference for timers
OutP	I	high-speed analog voltage	
OutN	I	high-speed analog voltage	
DisableIntReset	I	CMOS	Choose internal or external reset
ActivityOn	I	CMOS	pulse when activity is detected
ExternalResetP	I	CMOS	external reset
ExternalResetN	I	CMOS	external reset
EnableClk	I	CMOS	enable clock measurement
ResetP	O	CMOS	reset towards TIA
ResetN	O	CMOS	reset towards TIA
ResetP1	O	CMOS	reset for pos. pk. det. in stage 1
ResetN1	O	CMOS	reset for neg. pk. det in stage 1
ResetN2	O	CMOS	reset for neg. pk. det. in stage 2
ResetN3	O	CMOS	reset for neg. pk. det. in stage 3
ResetN4	O	CMOS	reset for neg. pk. det. in stage 4
DelayActDetect	O	CMOS	delays activity detect after reset
ClkMeas	O	CMOS clock	clock for timer trimming

Table 4.2: Reset block I/O

or an external reset.

4.6.1 Timer circuit and operation

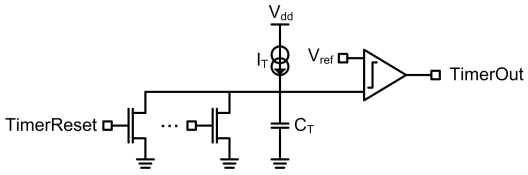

Figure 4.24: Timer circuit

Figure 4.24 shows the timer circuit. Each timer defines an elapsed time by charging capacitor C_T with a current I_T and comparing the resulting voltage with a reference V_{ref}. The timer is turned off and reset when one of the switches in parallel with C_T is closed. When all switches are open, the timer starts and TimerOut will become high if none of the switches closes during the elapsed time defined by the timer. Timer1, Timer2 and Timer7 have only one output. The

other timers have two complementary CMOS outputs. All timers use 490 fF as unit capacitance C_u and 278 uA as unit current I_u. The capacitances of all timers were laid out in a matched array. In this way mismatch between the capacitances is reduced and the capacitance corner deviation of all timers can be trimmed away by changing the reference voltage V_{ref}. The timer length is given by

$$\Delta T = C_T \frac{V_{ref}}{I_T}. \tag{4.31}$$

If we express the capacitance C_T as $n_C C_u$ and the current I_T as $n_I I_u$, then (4.31) becomes

$$\Delta T = V_{ref} \frac{n_C}{n_I} \cdot \frac{C_u}{I_u}. \tag{4.32}$$

Corner variations will cause C_u to vary over 30%. From Equation (4.32) it is clear that changing V_{ref} can trim away the capacitor corner variation. Table 4.3 gives the number of unit capacitances n_C and number of unit currents n_I used per timer.

Name	$\mathbf{n_C}$	$\mathbf{n_I}$	$\mathbf{\Delta T}$ **(ns)**
Timer1	8	3	7.9
Timer2	10	3	9.9
Timer3	3	2	4.4
Timer4	7	3	6.9
Timer5	2	2	3.0
Timer6	2	2	3.0
Timer7	9	2	13.3
TimerClk	3	1	8.9

Table 4.3: Configuration and duration of timers

4.6.2 Reset detection

Figure 4.25 shows the part of Figure 4.23 that is used for the end of burst detection. The outputs of the datapath are compared and converted to a CMOS signal R_{bit}. This signal is one of the four reset signals of Timer1. This timer measures the time since the last detected '1' because it is reset every time a '1' is received. If this time exceeds 8 ns it is assumed that the burst has ended. The second timer reset input is the ResetP output itself. This resets the timer ready for the next burst. To avoid multiple resets being generated during the guard time, signal EnReset is used. This signal is the output of Timer6 in Figure 4.23. This signal goes low when the preamble has finished, indicating that the reset detection functionality is required again. The reset detection is disabled during the preamble because the preamble can contain sequences triggering a reset pulse. The fourth reset input to

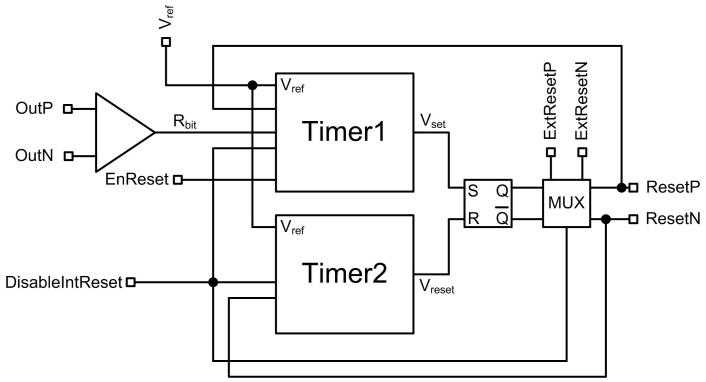

Figure 4.25: Reset circuit

Timer1 is DisableIntReset. When this signal is high, the internal reset detection mechanism is overridden for test purposes and an external reset signal is input to ExtResetP and ExtResetN.

Timer2 determines the length of the reset pulse. Its length needs to be sufficient to reset the PKDs on the TIA. This timer is started when a reset is detected indicated by ResetN becoming low. When Timer2 has ended, V_{reset} becomes high ending the reset pulse (ResetP and ResetN).

Signals ResetP and ResetN are converted into CML signals and sent to the TIA. On the BM-PA itself, the PKDs require reset signals that remain on until their respective preamble pattern has arrived. These reset signals are created by Timer3, Timer4, Timer5 and Timer6.

The time measured by the timers can deviate from the ideal time given by equation 4.31 due to process variations of C_T, offset of the timer comparator and comparator input capacitance and switch capacitances that add to the C_T value. This could lead to a false reset signal. One could of course take a margin on ΔT, but to keep this margin small, a trimming mechanism has been implemented. This mechanism will be explained in section 4.6.4.

4.6.3 Trimmable timer voltage reference

Figure 4.26 shows how the voltage reference V_{ref} is generated. A bandgap voltage V_{bg} is multiplied with a factor M and then buffered with an OTA. This reference voltage for the timer can be changed by setting the multiplication factor

$$M = (1 + \frac{R_2}{R_1}). \tag{4.33}$$

Figure 4.27 shows the simulated output voltage of the trimmable voltage reference for different values of M.

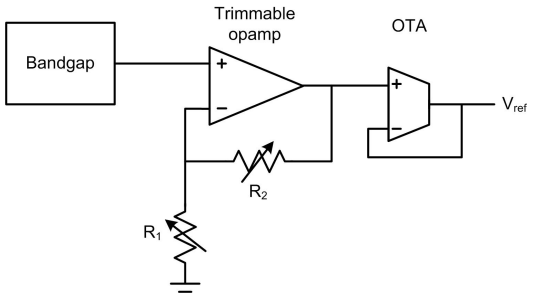

Figure 4.26: Trimmable voltage reference circuit

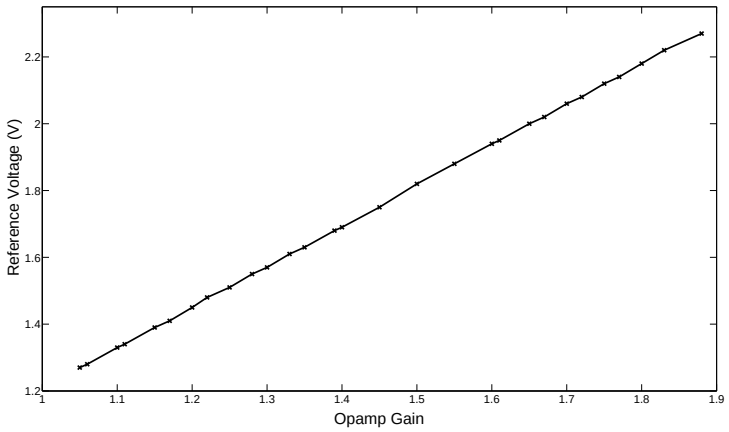

Figure 4.27: Simulated trimmable voltage reference output

4.6.4 Timer Trimming

In order to trim away the capacitance corner, one has to measure the capacitance somehow. A clock was generated on-chip for this purpose using two timers with equal length. This creates a clock with a typical period 19.3 ns. This clock period is given by (assuming the comparator input capacitance is negligible)

$$T_{clock} = 2V_{ref}\frac{n_C}{n_I} \cdot \frac{C_u}{I_u}. \tag{4.34}$$

Equation (4.34) illustrates that the unit capacitance value can be extracted from the clock period measurement. A test mode to measure the reference voltage is also implemented and the unit current is accurately generated by an external resistor with high accuracy. Because $T_{clock,meas} = T_{clock}$ the trimmed V_{ref} value is

calculated to be

$$V_{ref,trimmed} = V_{ref} \frac{C_u}{C_{meas}}. \tag{4.35}$$

Because

$$\frac{C_u}{C_{meas}} = \frac{T_{clock}}{T_{clock,meas}}, \tag{4.36}$$

Equation (4.35) can be written as

$$V_{ref,trimmed} = V_{ref} \frac{T_{clock}}{T_{clock,meas}}. \tag{4.37}$$

From Equation (4.37) the new resistor ratio $\frac{R_2}{R_1}$ can be calculated. It is clear that the process variation can be trimmed away, but other causes will still generate a systematic offset. Because of this offset and also because of mismatch, there is a possibility that a timer designed for 7.2 ns in typical case, measures a time shorter than 7.2 ns and hence generates the reset too soon, or generates a false reset. For this reason the reset timer was designed for 8 ns to avoid these erroneous reset signals. Simulations including the trimming were performed to ensure that in all cases, the ResetTimer measures a minimum time of 8 ns.

Figure 4.28 shows the measured clock outputs for 3 different settings of the trimmable opamp gain on the BM-PA. The upper trace (R2) shows the clock output for the minimum gain setting, the middle trace (R1) shows the clock output for the typical gain setting of the trimmable opamp gain, and the lower trace (R3) shows the clock output for the maximum gain setting. As can be seen from the figure, the clock period can be trimmed from 16.26 ns to 29.82 ns, which is a range of 60%. As the capacitance value can vary over $\pm$ 30% this proves that the trimming mechanism can effectively trim out the corner variations of the timer capacitance.

4.7 Burst Detection Implementation

The BM-PA also provides a burst envelope signal to the CDR. This function is implemented in the burst detection block. The burst detection circuitry cannot reduce sensitivity of the Rx, so usually its bandwidth is limited to reduce noise. If a reference is used to detect the start of a burst, the choice of this reference is very critical. It should be placed in such way that all bursts are detected and that the probability of seeing activity purely due to noise is minimal. This requires the knowledge of a reference below which no activity is present. On the TIA this would be the dark level (output of TIA core without input current). Due to the THE on the TIA, the minimum of the positive phase of a signal (or the maximum of the negative phase of the incoming signal) is unknown (without THE on the TIA, this minimum would be the common-mode level of the signal). Therefore there is no reference above which there certainly is activity. Because of the lack of such a

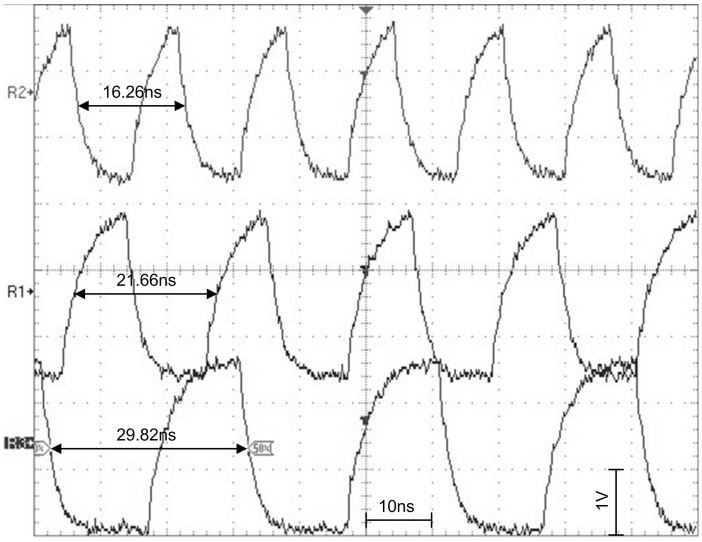

Figure 4.28: Measured on-chip clock

reference, the only way to detect the start of a burst is to detect edges. Figure 4.29 shows the burst detection architecture. The incoming signal is differentiated by means of a high-pass filter. Because the outputs of this differentiator can be very narrow pulses, the outputs are integrated again to make detection of the pulses easier. This is done by an amplifier with limited bandwidth. The output of the integrator is compared to a reference that is located slightly above the output of the integrator in absence of a signal.

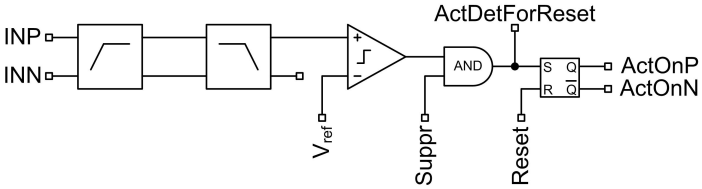

Figure 4.29: Burst detection block

The detection of bursts should be disabled during and shortly after the reset to avoid triggering the activity on the reset transients of the TIA. The signal $Suppr$ is low during reset and for a certain time after the end of the reset (this time is defined by Timer7). The AND port disconnects the comparator output from the latch during this period. The $ActDetForReset$ signal is used in the reset block for synchronizing the release of the resets for the different stages with the start of the burst. The latch converts the burst detect pulse into a burst envelope for the

CDR. ActOnP and ActOnN are CMOS signals so a CMOS-to-CML converter is added on chip (not shown in the drawing).

4.8 Packaging

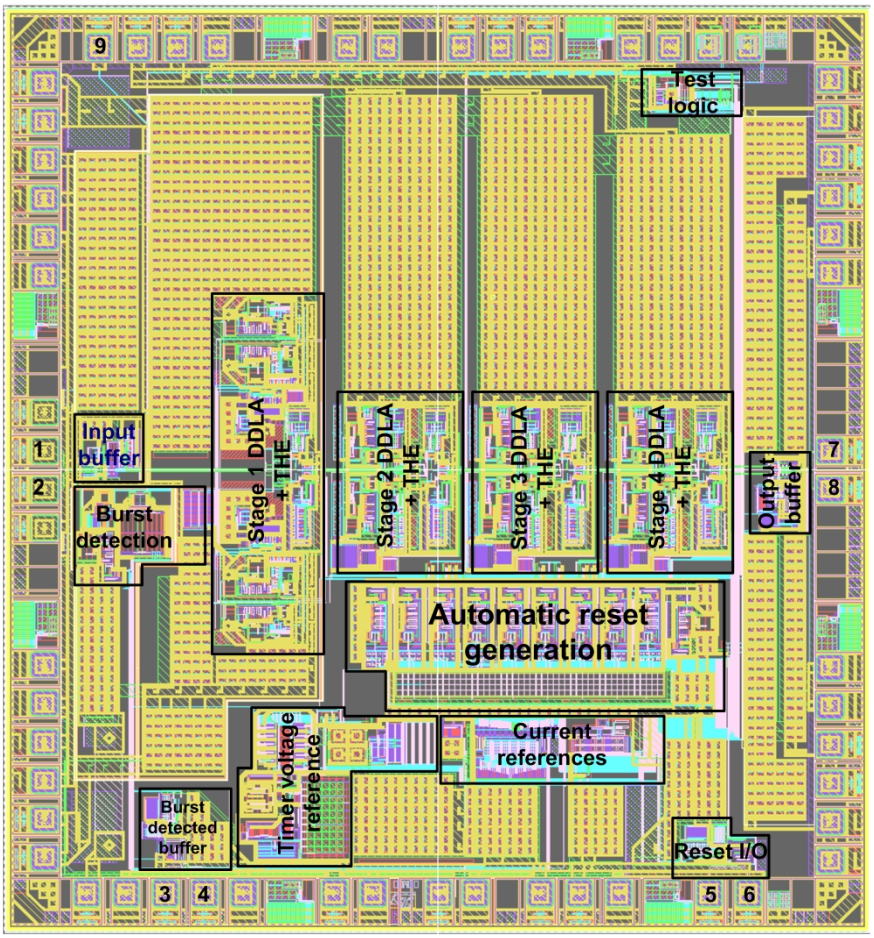

Figure 4.30: VAMB layout

Figure 4.30 shows the layout of the second version of the 10 Gb/s BM-PA called VAMB. It measures 2.3 mm by 2.5 mm. The first version was slightly smaller (2.1 mm by 2.1 mm) and did not include the burst detect functionality. The most important bond pads have been numbered. The BM-PA inputs (pad 1 and 2) are located at the left side of the die. The outputs (pad 7 and 8) were placed on the opposite side to reduce crosstalk between outputs and inputs. The outputs

of the input buffer are used for the burst detection circuitry. The main part of these circuits are placed close to the input buffer to reduce the capacitive load on the output traces of the input buffer. The burst detection block in the lower left corner includes a driver for the burst envelope signal. This burst detected signal is output through pads 3 and 4. The datapath was placed along the symmetry axis of the die. The reset detection block shows the timers and the matched array of capacitances. The burst detection buffer provides 50 Ω terminations for an incoming reset signal (if an external reset is applied for testing). If an internal reset is used the block acts as a driver for the reset signals output through pads 5 and 6. The external reference voltage for the burst detection circuits is applied through pad 9. As on the BM-TIA, a large number of decoupling capacitors was included on chip. These capacitors take up more than a quarter of the total die area.

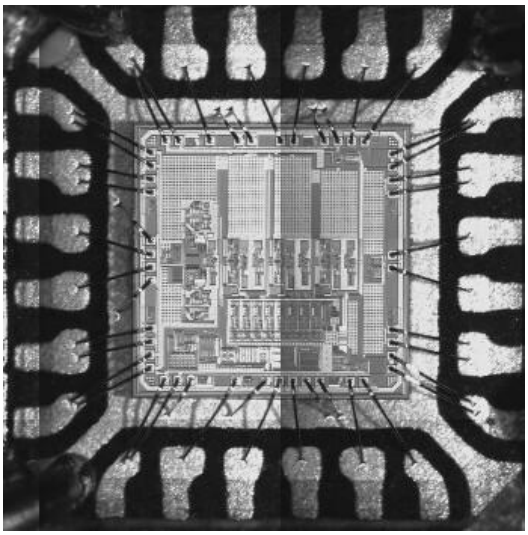

Figure 4.31: Packaged VAMA micrograph

The BM-PA was designed in a 0.25 μm SiGe BiCMOS technology and occupies 2.1 mm x 2.1 mm (VAMA) and 2.3 mm x 2.5 mm (VAMB). The first version of the limiting amplifier, VAMA, was integrated in a 4 mm by 4 mm MLF package from Amkor with 24 pins (Figure 4.31).

The second version, VAMB, with full functionality, was packaged in a 5 mm by 5 mm package with 32 pins (Figure 4.32). These MLF packages contain a big metallization plate at the bottom, which was used for downbonding ground connections. In this way, a very low ground impedance can be ensured, ideal for 10 G operations. Additional ground connections (Gnd1 and Gnd3 in version 1, and Gnd1 and Gnd7 in version 2) have been provided via the package pins itself for the following reasons:

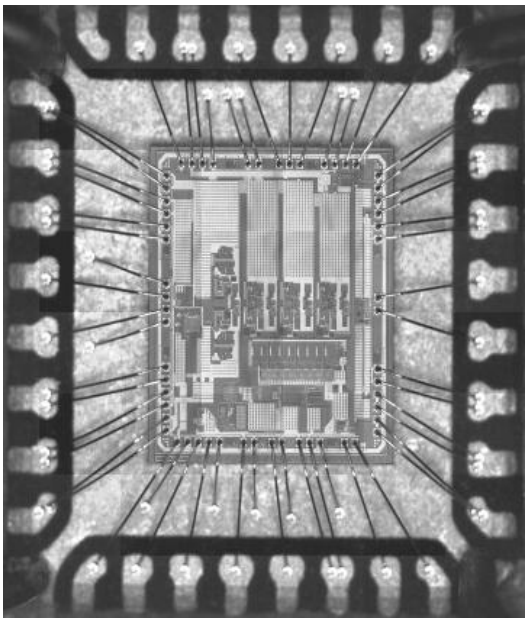

Figure 4.32: Packaged VAMB micrograph

- Reducing the amount of needed vias between power supply pins and decoupling capacitors
- Splitting grounds of input section and output section of the BM-PA.

The second version required more pins to accommodate extra supply domains. These extra domains were needed because the burst detect requires a 2.5 V supply towards the CDR, also, the output stage of the buffer needs to be terminated to 2.5 V for compatibility towards the CDR. The internal circuitry of activity detect and output buffer however still operates at 2.7 V. The division of the supply domains helps to reduce crosstalk.

To include the influence of bond wires into the simulations, the complete MLF package was modeled using FastHenry [27]. Mutual inductance between bond wires was taken into account as well as the capacitance between bond wires and ground plane.

4.9 Measurements

VAMA and VAMB respectively consume 1.1 W and 1.23 W. As this is larger than the 1 W maximum power consumption of the MLF packages, fans were used to keep the junction temperature below the maximum specification of the die. This

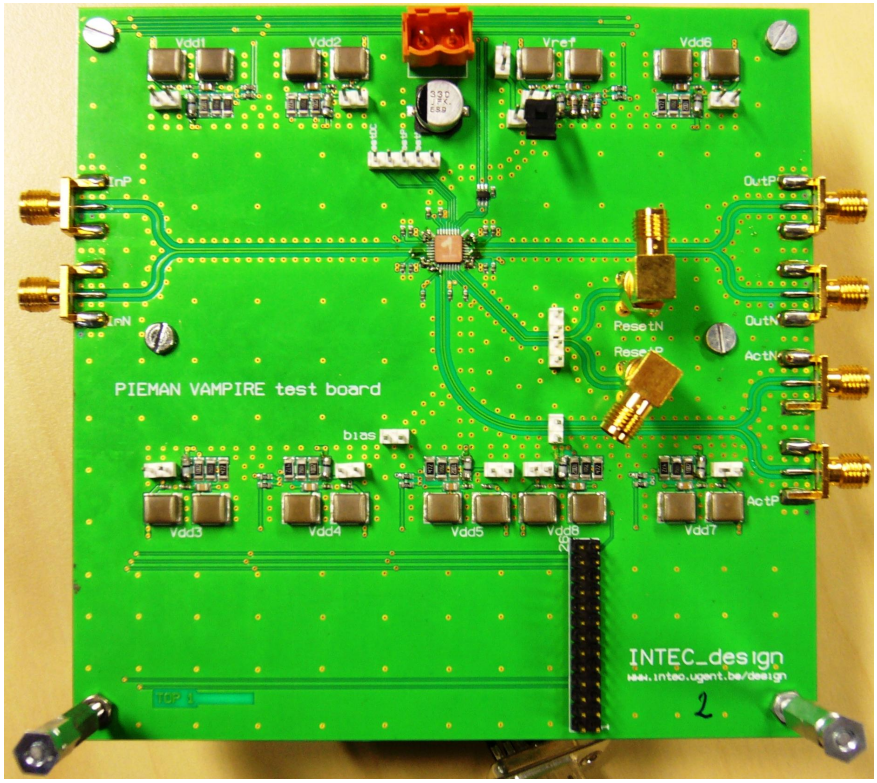

Figure 4.33: VAMB PCB

high power consumption has three main causes. Firstly, the comparators used in the PKDs need to switch quickly in order to limit the error on the detected peak, requiring large bias currents. As there are 10 PKDs on the BM-PA chip, the total power consumption of the peak detectors is about 150 mW. This is more than 10 % of the total power consumption. A second reason is that, because of the low supply voltage, a cascade of 2 complementary emitter followers has to be used (instead of only one voltage shifter) to buffer the large load resistance of the differential gain stages from the high input capacitance of the following stage and peak detector input. This is necessary to achieve high bandwidth. The charging and discharging of the large input capacitances requires high currents so the emitter followers are operated at rather high current levels. When using 4 stages to eliminate dc-offsets, the power consumption of the total BM-PA data path goes up quickly. Thirdly, the output buffer consumes a considerable amount of power (75 mW).

Figure 4.33 is a photograph of the PCB used for testing the 10 Gb/s BM-PA. Both input and output traces are 50 Ω transmission lines. The reset and burst detect interconnections were also designed as 50 Ω transmission lines. The test board

includes individual voltage regulators for each supply voltage domain so they can be set independently for testing. The reference for the burst detection is also generated with a similar voltage regulator. Like the BM-TIA test board, this board also includes a header for connecting a microcontroller. This microcontroller can then be used to set the supply voltages and internal BM-PA chip settings. A fan was mounted on the bottom side of the PCB to cool down the BM-PA package. This improved the performance of the BM-PA.

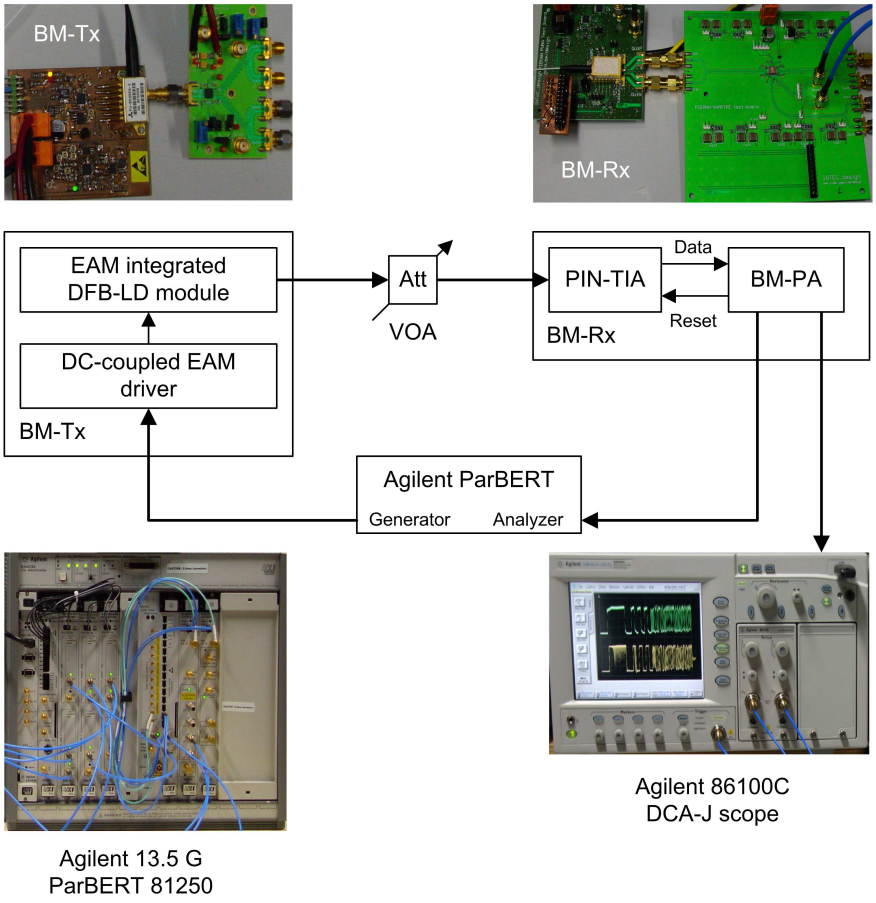

Figure 4.34: Back-to-back setup

The operation of the BM-PA can only be tested in combination with the BM-TIA as the test equipment is not capable of generating input signals with a differential offset. The first test setup is a back-to-back (B2B) configuration as shown in Figure 4.34. The 13.5 G data generator module of the Agilent ParBERT is used to generate the data signals to modulate the Electro-Absorption Modulator (EAM).

The dc-coupled EAM driver drives the EAM integrated distributed feedback laser laser diode (DFB-LD) module. This laser module outputs the optical signals that emulate the upstream traffic of one ONU in the PIEMAN network. A variable optical attenuator (VOA) is used to emulate the attenuation of the fiber in the optical network. In this way, the BM-Rx's sensitivity and overload can be tested. A 10-90 splitter was used for measuring the optical power arriving at the BM-Rx. The 10% fraction was sent to the optical power meter, while the other fraction was coupled to the BM-Rx. The outputs of the PIN BM-TIA were input to the BM-PA, the reset outputs of the BM-PA were fed back to reset the TIA. The outputs of the BM-PA were either viewed on the Agilent 86100C DCA-J scope, or input to the analyzer (ParBERT) to measure BERs. The Tx was built within INTEC_design with relatively low-cost off-the-shelf components. It was not optimized in terms of ER and modulation waveform at 10 Gb/s causing an extra BM penalty that was not observed when more expensive devices or instruments were used as Tx.

A high-speed sampling scope was used to test the advanced functionality like the reset and burst envelope generation. Figure 4.35 shows the BM-TIA output, BM-PA output, Reset and Burst Detected (burst envelope) signals. As explained, the Reset signal is sent to the TIA and the burst detect signal is sent to the CDR. The figure clearly shows that both the burst detection and automatic reset generation operate correctly. One can see that at the end of the burst, the reset is generated during the guard time. The burst envelope goes down some nanoseconds later. The effect of the reset is also clearly visible in the output of the BM-TIA. Some time after the start of the new burst, the burst envelope goes high again indicating that the new burst is detected by the BM-PA.

The setup in Figure 4.34 was used to test the B2B sensitivity and overload of the BM-Rx. The results at 5 Gb/s are shown in Figure 4.36 for 2.15 μs burst length, 25.6 ns guard time and 25.6 ns preamble. The payload was a PRBS $2^{31}-1$ sequence. These results were reported in [28]. The sensitivity and overload are summarized in Table 4.4. The Rx sensitivity was limited by the large bandwidth of the Rx because it was designed for 10 Gb/s operation. The burst detection circuitry was also designed for the minimum input optical input power of -16 dBm and thus it failed to operate correctly below that input power level.

The worst scenario for a BM-Rx is a strong burst immediately followed by a weak burst with only the minimum guard time in between. For these tests the setup with two Tx's from Figure 4.37 was used. A gated SOA was added to increase the optical output power of the 2^{nd} BM-Tx, in order to generate a sufficient loud/soft ratio for this experiment. In addition, an optical isolator (ISO) was inserted at the output of the SOA and an optical bandpass filter (OBPF) was used to reject the ASE noise of the SOA. To emulate the worst-case scenario, a strong packet generated by a low-speed generator (2.5 Gb/s) was followed by the weak high-speed packet (10 Gb/s) on which the BER was measured. This experiment was limited to

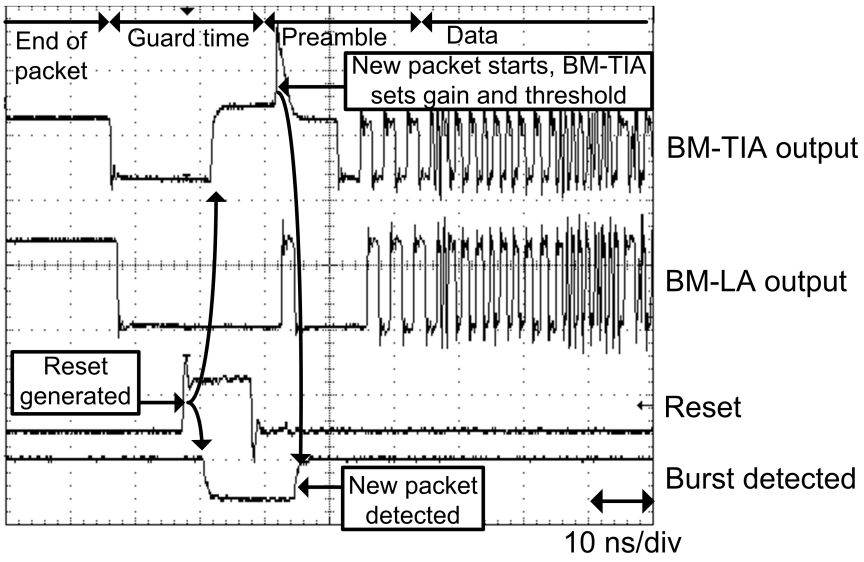

Figure 4.35: Measured automatic reset generation and burst detection waveforms

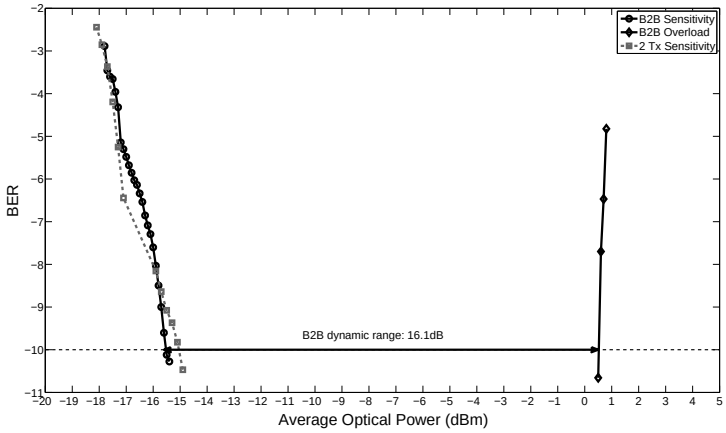

Figure 4.36: Measured BER results at 5 Gb/s

5 Gb/s because the 10 Gb/s and 2.5 Gb/s bursts could not be synchronized properly due to jitter on the 2.5 Gb/s clock. This clock is used to synchronize the 10 Gb/s module in the ParBERT. The results are also shown in Figure 4.36 and summarized in Table 4.4. These tests were performed with the same sequence of bursts as the B2B-tests. The BM penalty was 0.5 dB with a loud/soft ratio of 15.1 dB. The

5 Gb/s	**B2B**	**2 branches (L/S=15.1 dB)**	**remark**
Sensitivity (dBm, BER=1e-10)	-15.6	-15.1	BMRx sensitivity at 5 Gb/s is limited by BW>9GHz and burst detection
Overload (dBm)	+0.5	+0.5	
DR (dB)	16.1	15.6	on the same branch

Table 4.4: Summary of the measured uplink performance at 5 Gb/s

measured overload was 0.5 dBm so the dynamic range was 15.6 dB.

Figure 4.38 shows the outputs in the worst-case scenario for a loud/soft ratio of 12 dB. This measurement was performed at 10 Gb/s with a fixed PRBS pattern of $2^{11} - 1$ with added 72 consecutive '1's and '0's. As can be seen from that figure, the reset is visible in the outputs of the BM-PA as then the threshold information is erased. One can also see that while the optical input signal (upper trace) shows a large difference in amplitude, the amplitude of both bursts at the BM-PA outputs is the same.

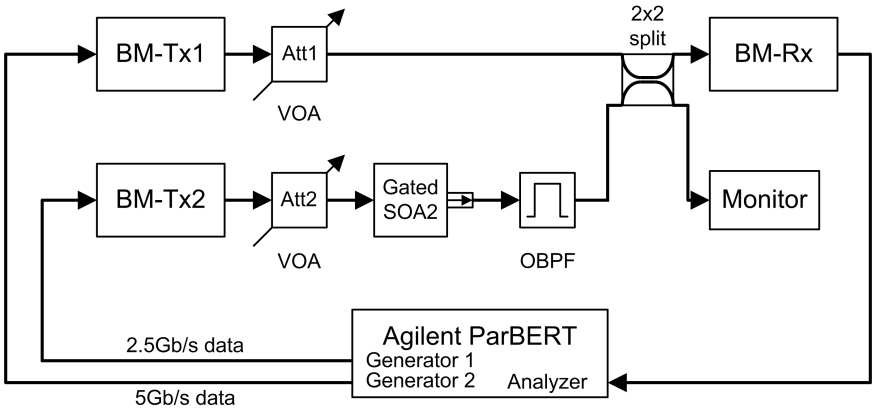

Figure 4.37: Setup with two transmitters

The B2B BER was also measured at 10 Gb/s. The results are given in Table 4.5 and the BER curve is shown in Figure 4.39. A PRBS $2^7 - 1$ was used for testing. The ER of BM-Tx2 was 7.5 dB during measurements. The measured BM-Rx sensitivity was - 10.5 dBm (BER=10^{-10}) when BM-Tx1 was used and - 13.4 dBm with the BM-Tx2, which had a better transmission performance. The measured overload was - 0.8 dBm (error free) respectively - 0.3 dBm. The dynamic

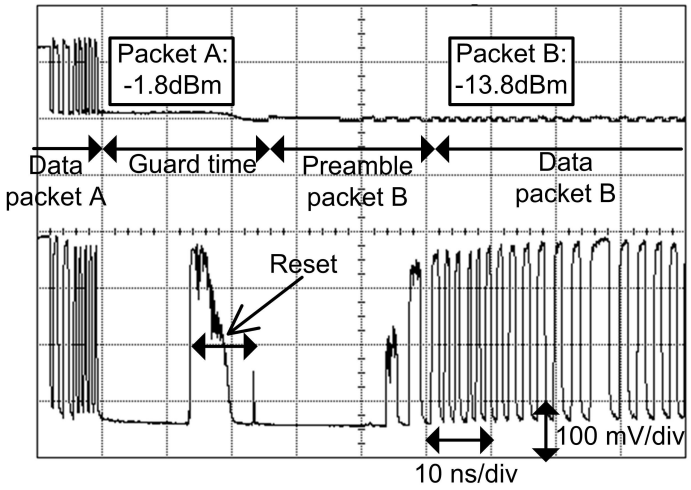

Figure 4.38: Optical input (upper trace) and electrical output (lower trace) for strong packet followed by weak packet [17]

range was more than 10 dB with BM-Tx1, and 13.1 dB with BM-Tx2.

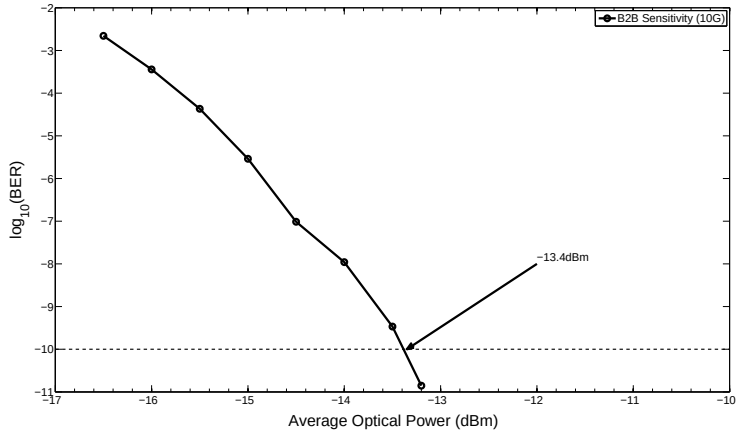

Figure 4.39: Measured B2B BER curves at 10 Gb/s

10 Gb/s	**B2B**
Sensitivity BM-Tx1 (dBm)	-10.5
Sensitivity BM-Tx2 (dBm)	-13.4
Overload (dBm)	-0.3
DR BM-Tx2 (dB)	13.1

Table 4.5: Summary of the measured uplink performance at 10 Gb/s

References

[1] T. De Ridder, P. Ossieur, C. Mélange, B. Baekelandt, J. Bauwelinck, X. Z. Qiu, and J. Vandewege. *10 Gbit/s burst-mode post-amplifier with automatic reset*. Electronics Letters, 44(23):1371+, Nov. 6 2008.

[2] B. Baekelandt, J. Bauwelinck, T. De Ridder, Ossieur P. Mélange, C., X.-Z. Qiu, and J. Vandewege. *Device and method for signal detection in a TDMA network*, May 2009.

[3] P. Ossieur, T. De Ridder, J. Bauwelinck, E. De Backer, J. Gillis, X. Z. Qiu, and J. Vandewege. *1.25 Gbit/s ITU-T G.984.2 burst-mode transimpedance amplifier without reset pins*. Electronics Letters, 43(18):991–993, Aug. 31 2007.

[4] P. Ossieur, T. De Ridder, J. Bauwelinck, X.-Z. Qiu, and J. Vandewege. *Systems and Methods for Transferring Single-Ended Burst Signal onto Differential Lines, Especially for Use in Burst-Mode Receiver*, Oct. 2006.

[5] *Gigabit-capable Passive Optical Networks (GPON): Physical Media Dependent (PMD) layer specification*. ITU-T Recommendation G.984.2.

[6] K. Hara, S. Kimura, H. Nakamura, N. Yoshimoto, M. Tsubokawa, K. Nishimura, M. Nakamura, and S. Nishihara. *A 1.25/10.3-Gbit/s ac-coupled dual-rate burst-mode receiver without reset signals*. In 2008 34th European Conference on Optical Communication (ECOC 2008), page 2 pp., Sept. 2008.

[7] S. Vatannia, P.H. Yeung, and C. Lu. *A fast response 155-Mb/s burst-mode optical receiver for PON*. IEEE Photonics Technology Letters, 17(5):1067–1069, May 2005.

[8] Q. Le, S.G. Lee, Y.H. Oh, H.Y. Kang, and T.H. Yoo. *A burst-mode receiver for 1.25-Gb/s ethernet PON with AGC and internally created reset signal*. IEEE Journal of Solid-State Circuits, 39(12):2379–2388, Dec. 2004. IEEE International Solid-State Circuits Conference (ISSCC 2004), San Francisco, CA, Feb., 2004.

[9] Y. Ota, R.G. Swartz, V.D. Archer, S.K. Korotky, M. Banu, and A.E. Dunlop. *High-speed, Burst-mode, Packet-Capable Optical Receiver and Instantaneous Clock Recovery For Optical Bus Operation*. Journal of Lightwave Technology, 12(2):325–331, Feb. 1994. OFC/IOOC 93 Workshop on ICs for Lightwave Communications, SAN JOSE, CA, Feb. 21, 1993.

[10] Y. Ota and R.G. Swartz. *Burst-mode compatible optical receiver with a large dynamic-range*. Journal of Lightwave Technology, 8(12):1897–1903, Dec. 1990.

[11] M. Nakamura, N. Ishihara, Y. Akazawa, and H. Kimura. *An Instantaneous Response CMOS Optical Receiver IC with Wide Dynamic-Range and Extremely High-Sensitivity Using Feedforward Auto-Bias Adjustment*. IEEE Journal of Solid-State Circuits, 30(9):991–997, Sept. 1995.

[12] T. den Bakker, K.Y. Tu, and Y.K. Park. *Decision threshold based on dynamic offset compensation for burst mode receiver*. In ECOC'01: 27th European Conference On Optical Communication, Vols 1-6, pages 222–223, 2001. 27th European Conference on Optical Communication (ECOC 01), Amsterdam, Netherlands, Sept. 30-Oct. 04, 2001.

[13] P. Ossieur, Y.C. Yi, J. Bauwelinck, X.Z. Qiu, J. Vandewege, and E. Gilon. *DC-coupled 1.25 Gbit/s burst-mode receiver with automatic offset compensation*. Electronics Letters, 40(7):447–448, Apr. 1 2004.

[14] P. Ossieur, D. Verhulst, Y. Martens, W. Chen, J. Bauwelinck, X.Z. Qiu, and J. Vandewege. *A 1.25-Gb/s burst-mode receiver for GPON applications*. IEEE Journal of Solid-State Circuits, 40(5):1180–1189, May 2005.

[15] S Brigati, P Colombara, L D'Ascoli, U Gatti, T Kerekes, and P Malcovati. *A SiGeBiCMOS burst-mode 155-Mb/s receiver for PON*. IEEE Journal of Solid-State Circuits, 37(7):887–894, Jul. 2002. 27th European Solid-State Circuits Conference (ESSCIRC), VILLACH, AUSTRIA, Sept. 18-20, 2001.

[16] P. Ossieur. *Ontwerp en modellering van burst-mode ontvangers voor Gigabit Passieve Optische Netwerken*. PhD thesis, Jun. 2005.

[17] P. Ossieur, T. De Ridder, J. Bauwelinck, C. Mélange, B. Baekelandt, Xing-Zhi Qiu, J. Vandewege, G. Talli, C. Antony, P. Townsend, and C. Ford. *A 10 Gb/s burst-mode receiver with automatic reset generation and burst detection for extended reach PONs*. In 2009 Conference on Optical Fiber Communication - OFC 2009, page 3 pp., Piscataway, NJ, USA, Mar. 2009. IEEE. 2009 Conference on Optical Fiber Communication - OFC 2009, 22-26 Mar. 2009, San Diego, CA, USA.

[18] P. Ossieur, X.Z. Qiu, J. Bauwelinck, and J. Vandewege. *Sensitivity penalty calculation for burst-mode receivers using avalanche photodiodes*. Journal of Lightwave Technology, 21(11):2565–2575, Nov. 2003.

[19] C.A. Eldering. *Theoretical Determination of Sensitivity Penalty For Burst Mode Fiber Optic Receivers*. Journal of Lightwave Technology, 11(12):2145–2149, Dec. 1993.

[20] P. Menendez-Valdes. *Performance of Optical Direct Receivers Using Noise-Corrupted Decision Threshold*. Journal of Lightwave Technology, 13(11):2202–2214, Nov. 1995.

[21] M.S. Leeson. *Calculation of sensitivity penalty for optically preamplified burst mode receivers using Fabry-Perot filters*. Electronics Letters, 34(11):1121–1122, May 28 1998.

[22] A. Papoulis. *Probability, Random Variables, and Stochastic Processes*. New York: McGraw-Hill, 1991.

[23] *MicroLeadFrame (MLF) QFN Package Datasheet*. `http://www.amkor.com/`.

[24] M. Nakamura, Y. Imai, Y. Umeda, J. Endo, and Y.J. Akatsu. *1.25-Gb/s burst-mode receiver ICs with quick response for PON systems*. IEEE Journal of Solid-State Circuits, 40(12):2680–2688, Dec. 2005. IEEE International Solid-State Circuits Conference (ISSCC 2005), San Francisco, CA, Feb. 06-10, 2005.

[25] P. Ossieur. *New concept for a gigabit burst-mode receiver, Internal report*. Dec. 2004.

[26] A. Neugroschel, C.T. Sah, and M.S. Carroll. *Degradation of bipolar transistor current gain by hot holes during reverse emitter-base bias stress*. IEEE Transactions on Electron Devices, 43(8):1286–1290, Aug. 1996.

[27] *FastHenry*. `http://www.fastfieldsolvers.com/`.

[28] X. Yin, X.Z. Qiu, B. Baekelandt, C. Mélange, T. De Ridder, J. Bauwelinck, and J. Vandewege. *5 Gbit/s burst-mode experiments for high split extended reach PONs*. Electronics Letters, 46(1):54–5, 7 Jan. 2010.

5 Conclusions and Further Research

In this final chapter the most important results of the research are highlighted. Suggestions for further research are given where possible, and one aspect of the ongoing research is mentioned more in detail.

5.1 Results

In this dissertation the design of a BM-Rx for 10 Gb/s extended reach PON was covered. A 10 Gb/s BM-TIA and BM-PA have been designed. The BM-TIA features a sophisticated gain locking mechanism that locks the gain within 4.5 ns. This avoids burst loss due to late gain switching decisions. The total run-in time of the 10 Gb/s BM-TIA is 6 ns. This is the shortest run-in time ever reported [1]. The BM-PA takes the inputs of the BM-TIA, removes offsets and amplifies the signals to CML-levels ready for the BM-CDR to perform the clock phase alignment. The 10 Gb/s BM-PA also incorporates burst detection and automatic reset generation. These circuits provide a burst envelope signal to the BM-CDR and a reset to the BM-TIA. This advanced functionality implies that no critical timing alignments are needed for operation or testing, and simplifies the design of the OLT. The response time of the BM-PA is 23.6 ns. The complete BM-Rx supports a minimum guard time of 25.6 ns. The guard time and preamble length are both the shortest ever published for such a BM-Rx [1]. Moreover, to achieve efficient network transmission and high interoperability, no time-critical control signals cross the boundary between the PON physical layer and the MAC layer.

Parameter	Value	Unit	Remark
Bit-rate	5/10	Gb/s	Dual rate possible
TIA preamble	6	ns	
PA preamble	23.6	ns	
Total preamble	29.6	ns	
Sensitivity @ 5 Gb/s	-15.1	dBm	BER = 10^{-10}, 2Tx
Sensitivity @ 10 Gb/s	-13.4	dBm	BER = 10^{-10}, B2B
Overload @ 5 Gb/s	+0.5	dBm	
Overload @ 10 Gb/s	-0.3	dBm	
Dynamic range @ 5 Gb/s	15.6	dB	
Dynamic range @ 10 Gb/s	13.1	dB	
TIA power consumption	0.6	W	
LA power consumption	1.3	W	
supply voltage	2.7	V	

Table 5.1: Final achieved specifications

Based on the PIEMAN uplink architecture, the BM-Rx input level was originally specified as -13 dBm. The DR was specified at 15 dB. During the project it became clear that the combination of the short overhead and automatic reset generation requirement was very challenging and that it had its repercussion on the receiver performance. Therefore, the PIEMAN consortium increased the BM-Rx input level to -10 dBm to -11 dBm at an OSNR of 20 dB. This can easily be done by increasing the gain of the preamplifying EDFA at the SN. The DR requirement was reduced to 10 dB, which can be achieved by ONU power levelling, as the gain of the postamplifying SOA at the ONU can be switched more than 5 dB conveniently. From this we can conclude that the designed BM-Rx fulfills all the requirements to perform correctly in the PIEMAN network.

The feasibility of the PIEMAN network was successfully demonstrated and the results of uplink tests with the designed BM-Rx were reported in several international conferences and in a journal [1–5].

5.2 Further Research

5.2.1 Improvements to the PIEMAN BM-PA

5.2.1.1 Threshold scaling

The feedforward configuration was found to be the only possible configuration given the constraints on power consumption, run-in time, power supply and chosen technology. The drawbacks of this configuration are a large BM penalty, a fixed slicing factor resulting in extra penalty, and a difficult internal reset timing

and alignment with the preamble. These problems can only be solved by either using a different technology that allows the use of traditional peak detectors (so a technology with other HBTs or small diodes and a larger supply voltage) or by allowing a longer run-in time.

Next generation PON systems are currently being standardized by both the IEEE EPON community (aiming for a symmetric 10 GE-PON (IEEE 802.3av) system) and the ITU-T FSAN study group for ITU-T XG-PON systems (10 Gb/s downstream and 2.5 Gb/s or 10 Gb/s upstream [1]). There seems to be significant industry support for aligning the 10 Gb/s optics of ITU-T XG-PON systems with the optical layer specification of IEEE 10 GE-PON systems. So both standards tend to longer overhead times than the 60 ns achieved by the PIEMAN BM-Rx. A run-in time of several hundred nanoseconds would allow a feedback configuration for the BM-PA, thereby enabling easier and more accurate threshold extraction. This also simplifies the implementation of a slicing factor different to 0.5 hence reducing the BM penalty.

5.2.1.2 Automatic reset generation

One drawback of the reset detection circuit is the CMOS reset signal of the timer. The output of the datapath is compared and converted to a CMOS signal to reset the timer. CMOS logic and switches are too slow to discharge the timer capacitance within one bit period. Therefore, the capacitance is not completely discharged during a data sequence with a high frequency of bit transitions. The charge and voltage on the capacitor keeps rising during these sequences and eventually a false reset might be generated. The solution to this problem is to generate a longer pulse every time a '1' is detected. This can easily be implemented with a monostable multivibrator.

5.2.1.3 BM-PA supply domains

The 10 Gb/s BM-PA chip has 8 different power supply domains requiring a lot of input pads. This high number of supply domains was chosen because different circuits require different supply voltages. The input buffer operates at the same supply voltage as the output buffer of the 10 Gb/s BM-TIA. During testing, these supplies were kept the same. The internal circuitry of the PA operates at 2.7 V. The output buffer needs a 2.5 V because the BM-CDR input buffer is terminated to 2.5 V. The same is true for the driver of the burst envelope signal. The output buffer shown in Figure 5.1 provides a different termination voltage to V_{cc} set by resistor $R1$. With this buffer the supply voltage of all output buffers can be the same 2.7 V supply as for the internal circuitry. The drawback is a reduced common-mode output return loss. This is not problematic as long as the input return loss of the BM-CDR input buffer is sufficient.

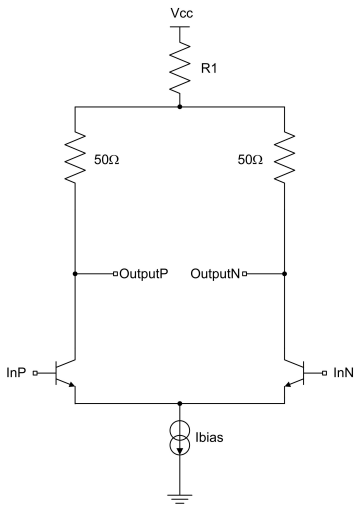

Figure 5.1: Modified output buffer circuit

5.3 M-switching

One direction of the future research is a 10 Gb/s APD-TIA module with a combination of TIA gain switching and APD M-switching. As mentioned in section 3.3.4, switching M is also a solution to increase the dynamic range. In the EU-funded FP7 ICT project MARISE, the aim is to design an APD-TIA with 21 dB dynamic range. For this, a very 'performant' APD is designed by the project partners with a gain-bandwidth product exceeding 160 GHz. This enables a large M-switch ratio while maintaining the bandwidth of the APD. This increases the DR with a factor

$$\frac{M_{max}}{M_{min}}, \tag{5.1}$$

M_{max} being the maximum APD gain and M_{min} the minimum APD gain.

The challenges in this project are the fast adaptation ($<$200 ns) of the APD reverse bias to avoid damaging the APD and the combination of both types of gain switching. Because the settling of the APD reverse bias after a voltage drop takes up most part of the preamble, and the settling time is unknown, the TIA gain is switched first.

A second direction for the future is the design of burst-mode receivers fulfilling the stringent requirements of the future standards. As explained in [1], this is a future direction for the INTEC_design lab.

References

[1] X.Z. Qiu, C. Mélange, T. De Ridder, B. Baekelandt, J. Bauwelinck, X. Yin, and J. Vandewege. *Evolution of burst mode receivers*. In 2009 35th European Conference on Optical Communication (ECOC), page 4 pp., Sept. 2009.

[2] P. Ossieur, T. De Ridder, J. Bauwelinck, C. Mélange, B. Baekelandt, Xing-Zhi Qiu, J. Vandewege, G. Talli, C. Antony, P. Townsend, and C. Ford. *A 10 Gb/s burst-mode receiver with automatic reset generation and burst detection for extended reach PONs*. In 2009 Conference on Optical Fiber Communication - OFC 2009, page 3 pp., Piscataway, NJ, USA, Mar. 2009. IEEE. 2009 Conference on Optical Fiber Communication - OFC 2009, 22-26 Mar. 2009, San Diego, CA, USA.

[3] X. Yin, X.Z. Qiu, B. Baekelandt, C. Mélange, T. De Ridder, J. Bauwelinck, and J. Vandewege. *5 Gbit/s burst-mode experiments for high split extended reach PONs*. Electronics Letters, 46(1):54–5, 7 Jan. 2010.

[4] P. Ossieur, C. Antony, A. Naughton, A. Clarke, P.D. Townsend, H.G. Krimmel, T. De Ridder, X.Z. Qiu, C. Mélange, A. Borghesani, D. Moodie, A. Poustie, R. Wyatt, B. Harmon, I. Lealman, G. Maxwell, D. Rogers, and D. Smith. *A Symmetric 320Gb/s Capable, 100km Extended Reach Hybrid DWDM-TDMA PON*. In 2010 Conference on Optical Fiber Communication - OFC 2010, page 3 pp., Mar. 2010. 2010 Conference on Optical Fiber Communication - OFC 2010, 21-25 March 2010, San Diego, CA, USA.

[5] C. Mélange, X. Yin, B. Baekelandt, T. De Ridder, X.Z. Qiu, J. Bauwelinck, J. Gillis, P. Demuytere, and J. Vandewege. *Fully DC-Coupled 10Gb/s Burst-Mode PON Prototypes and Upstream Experiments with 58ns Overhead*. In 2010 Conference on Optical Fiber Communication - OFC 2010, page 3 pp., Mar. 2010. 2010 Conference on Optical Fiber Communication - OFC 2010, 21-25 March 2010, San Diego, CA, USA.

List of Publications

Publications in international journals

- X. Yin, X.Z. Qiu, B. Baekelandt, C. Mélange, **T. De Ridder**, J. Bauwelinck, J. Vandewege, "5 Gbit/s burst-mode experiments for high split extended reach PONs", Electronics Letters, 46(1):54-55, JAN 2010.

- C. Mélange, B. Baekelandt, J. Bauwelinck, P. Ossieur, **T. De Ridder**, X.Z. Qiu, J. Vandewege, "Burst-Mode CDR Performance in Long-Reach High-Split Passive Optical Networks", Journal of Lightwave Technology, 27(17): 3837-3844, SEP 2009.

- X. Yin, J. Bauwelinck, **T. De Ridder**, P. Ossieur, X.Z. Qiu, J. Vandewege, O. Chasles, A. Devos, P. De Pauw, "Design of Automotive VCSEL Transmitter with On-Chip Feedforward Optical Power Control", IEICE Transactions on Electronics, E92C(9), SEP 2009.

- P. Ossieur, J. Bauwelinck, X. Yin, C. Mélange, B. Baekelandt, **T. De Ridder**, X.Z. Qiu, J. Vandewege, "A dual-rate burst-mode bit synchronization and data recovery circuit with fast optimum decision phase calculation", AEU-International Journal of Electronics and Communications, 63(11), 2009.

- C. Mélange, B. Baekelandt, P. Demuytere, J. Bauwelinck, K. Van Renterghem, **T. De Ridder**, X.Z. Qiu, J. Vandewege, "Mixed analogue/digital phase picking algorithm in oversampling burst-mode clock phase alignment", Electronics Letters, 45(13):694-695, JUN 2009.

- B. Baekelandt, C. Mélange, J. Bauwelinck, P. Ossieur, **T. De Ridder**, X.Z. Qiu, J. Vandewege, G. Talli,"Polarization Dependence of Linear In-Band Crosstalk in Multipoint-to-Point Networks", IEEE Photonics Technology Letters, 21(6):398-400, MAR 2009.

- **T. De Ridder**, P. Ossieur, C. Mélange, B. Baekelandt, J. Bauwelinck, X.Z. Qiu, J. Vandewege,"10 Gbit/s burst-mode post-amplifier with automatic reset", Electronics Letters, 44(23):1371-1372, NOV 2008.

- P. Ossieur, C. Mélange, **T. De Ridder**, J. Bauwelinck, B. Baekelandt, X.Z. Qiu, J. Vandewege,"Burst-Mode Electronic Equalization for 10-Gb/s Passive Optical Networks", IEEE Photonics Technology Letters, 20(17-20): 1706-1708, SEP-OCT 2008.
- B. Baekelandt, C. Mélange, J. Bauwelinck, P. Ossieur, **T. De Ridder**, X.Z. Qiu, J. Vandewege,"OSNR penalty imposed by linear in-band crosstalk caused by interburst residual power in multipoint-to-point networks", IEEE Photonics Technology Letters, 20(5-8):587-589, MAR-APR 2008.
- **T. De Ridder**, P. Ossieur, X. Yin, B. Baekelandt, C. Mélange, J. Bauwelinck, X.Z. Qiu, J. Vandewege,"BiCMOS variable gain transimpedance amplifier for automotive applications", Electronics Letters, 44(4):287-288, FEB 2008.
- X. Yin, P. Ossieur, **T. De Ridder**, J. Bauwelinck, X.Z. Qiu, J. Vandewege, "An improved current-mode squarer/divider circuit for automotive applications", IEICE Transactions on Electronics, E91C(2):232-234, FEB 2008.
- P. Ossieur, **T. De Ridder**, J. Bauwelinck, E. De Backer, J. Gillis, X.Z. Qiu, J. Vandewege, "1.25 Gbit/s ITU-T G.984.2 burst-mode transimpedance amplifier without reset pins", Electronics Letters, 43(18):991-993, AUG 2007.
- P. Ossieur, **T. De Ridder**, X.Z. Qiu, J. Vandewege, "Influence of random DC offsets on burst-mode receiver sensitivity", Journal of Lightwave Technology, 24(3):1543-1550, MAR 2006.

Publications in international conference and symposium proceedings

- P. Townsend, P. Ossieur, C. Antony, A. Naughton, A. M. Clarke, R. P. Davey, H.G. Krimmel, **T. De Ridder**, X.Z. Qiu, C. Melange, A. Borghesani, D. Moodie, A. Poustie, R. Wyatt, B. Harmon, I. Lealman, G. Maxwell, D. Rogers, D. W. Smith, S. Smolorz, "European Research Project PIEMAN" to be published in Access Networks and In-house Communications (ANIC) conference, 2010, Karlsruhe.
- C. Mélange, X. Yin, B. Baekelandt, **T. De Ridder**, X.Z. Qiu, J. Bauwelinck, J. Gillis, P. Demuytere, J. Vandewege, "Fully DC-Coupled 10Gb/s Burst-Mode PON Prototypes and Upstream Experiments with 58ns Overhead", published in the 2010 Conference on Optical Fiber Communication - OFC 2010, 21-25 March 2010, San Diego, CA, USA.
- P. Ossieur, C. Antony, A. Naughton, A. Clarke, P.D. Townsend, H.G. Krimmel, **T. De Ridder**, X.Z. Qiu, C. Mélange, A. Borghesani, D. Moodie, A.

Poustie, R. Wyatt, B. Harmon, I. Lealman, G. Maxwell, D. Rogers, D. Smith, "A Symmetric 320Gb/s Capable, 100km Extended Reach Hybrid DWDM-TDMA PON", published in the 2010 Conference on Optical Fiber Communication - OFC 2010, 21-25 March 2010, San Diego, CA, USA.

- X.Z. Qiu, C. Mélange, **T. De Ridder**, B. Baekelandt, J. Bauwelinck, X. Yin, J. Vandewege, "Evolution of burst mode receivers", published in the 2009 35th European Conference on Optical Communication (ECOC), Vienna, 2009, invited paper, pp. 7.5.1.

- S. Smolorz, H. Rohde, P. Ossieur, C. Anthony, P. Townsend, **T. De Ridder**, B. Baekelandt, X.Z. Qiu, S. Appathurai, H.G. Krimmel, D. Smith, A. Poustie,"Next generation access networks: PIEMAN and beyond", published in the International Conference on Photonics in Switching 2009 Pisa, Italy, SEP 15-19, 2009.

- P. Ossieur, **T. De Ridder**, C. Antony, C. Melange, B. Baekelandt, X.Z. Qiu, C. Ford and P. D. Townsend, "Demonstration of a 5-Gb/s burst-mode receiver for optically amplified PON systems", Photonics Ireland 2009 Conference, Poster A45, 14-16, Sept. 2009, Kinsale, Ireland.

- J. Bauwelinck, C. Mélange, X. Yin, B. Baekelandt, T. De Ridder, X.Z. Qiu and J. Vandewege, "Research and development of wireline and wireless physical layer components and subsystems", European workshop on photonic solutions for wireless, access, and in-house networks (on CD-ROM), May, 18-20, 2009, Duisburg, Germany.

- P. Ossieur, **T. De Ridder**, J. Bauwelinck, C. Mélange, B. Baekelandt, X.Z. Qiu, J. Vandewege, G. Talli, C. Anthony, P. Townsend, C. Ford, "A 10 Gb/s burst-mode receiver with automatic reset generation and burst detection for extended reach PONs", published in the 2009 Conference on Optical Fiber Communication - OFC 2009, 22-26 March 2009, San Diego, CA, USA.

- **T. De Ridder**, P. Ossieur, B. Baekelandt, C. Mélange, J. Bauwelinck, C. Ford, X.Z. Qiu, J. Vandewege, "A 2.7 V 9.8 Gb/s burst-mode TIA with fast automatic gain locking and coarse threshold extraction", published in the 2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, 3-7 February 2008, San Francisco, CA, USA.

- P. Townsend, G. Talli, C.W. Chow, E.M. MacHale, C. Anthony, R. Davey, **T. De Ridder**, X.Z. Qiu, P. Ossieur, H.G. Krimmel, D. Smith, I. Lealman, A. Poustie, S. Randel, H. Rohde,"Long reach passive optical networks", published in 2007 IEEE LEOS ANNUAL MEETING CONFERENCE PROCEEDINGS, VOLS 1 AND 2, Lake Buena Vista, FL, OCT 21-25, 2007.

- R. Davey, **T. De Ridder**, X.Z. Qiu, P. Ossieur, H.G. Krimmel, D. Smith, I. Lealman, A. Poustie, G. Talli, C.W. Chow, P. Townsend, S. Randel, H. Rohde, "Progress in IST project PIEMAN towards a 10 Gbit/s, multiwavelength long reach PON", published in Broadband Europe 2006, Geneva, Switzerland, DEC 2006.

- X.Z. Qiu, Y.C. Yi, P. Ossieur, S. Verschuere, D. Verhulst, B. De Mulder, W. Chen, J. Bauwelinck, **T. De Ridder**, B. Baekelandt, C. Mélange, J. Vandewege, "High performance burst-mode upstream transmission for next generation PONs", published in 2006 Asian Optical Fiber Communication & Optoelectronic Exposition and Conference.

Publications in national conference and symposium proceedings

- **T. De Ridder**, X.Z. Qiu, J. Vandewege, "10 Gbit/s Burst-mode Receivers for Next Generation PONs", 10th FTW PHD Symposium, Interactive poster session, 9 December 2009, Ghent , Belgium.

- **T. De Ridder**, X. Yin, P. Ossieur, X.Z. Qiu, J. Vandewege, O. Chasles, A. Devos, P. De Pauw, "Monolithic Transimpedance Amplifier Design for Large Photodiode Capacitance and Wide Temperature Range", published in the Proceedings of the 10th Annual Symposium of the IEEE/LEOS Benelux Chapter 2005, 1-2 December 2005, Mons , Belgium , pp. 245-248.

- X. Yin, D. Verhulst, J. Bauwelinck, **T. De Ridder**, P. Ossieur, X.Z. Qiu, J. Vandewege, O. Chasles, A. Devos, P. De Pauw, "A Novel Automotive VCSEL Driver with Feed-Forward Bias and Modulation Current Control", published in the Proceedings of the 10th Annual Symposium of the IEEE/ LEOS Benelux Chapter 2005, 1-2 December 2005, Mons , Belgium , pp. 241-244.

- **T. De Ridder**, P. Ossieur, X.Z. Qiu, J. Vandewege, "Burst-mode Receivers for Long-reach Amplied Optical Networks at 10 Gbit/s", 7th FTW PHD Symposium, Interactive poster session, 29 November 2009, Ghent , Belgium.

Patents

- B. Baekelandt, J. Bauwelinck, **T. De Ridder**, C. Mélange, P. Ossieur, X.Z. Qiu, J. Vandewege,"Device and method for signal detection in a TDMA network", International published number WO 2009 065861 A2, on 28 May

2009; and United States Application Serial Number 12/680,011, Case No.: 07-1159-WO-US, March 25, 2010.

- J. Bauwelinck, **T. De Ridder**, P. Ossieur, X.Z. Qiu, J. Vandewege,"Systems and Methods for Transferring Single-Ended Burst Signal onto Differential Lines, Especially for Use in Burst-Mode Receiver", International Patent PCT/EP2006/067215, 9 October 2006.